Fundamentals of Analog & Mixed Signal VLSI Design
Exercise 5 (16.10.2024)

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In this exercise we want to apply the G_m/I_D design methodology using the inversion coefficient IC to the simple common source amplifier shown in Fig. 1 for various specifications. For the design we assume a generic 180 nm CMOS process with the parameters given in Table 1.

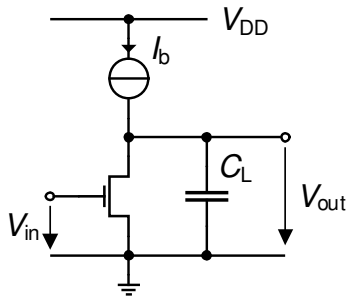

Figure 1: Common source amplifier.

Table 1: Technology parameters of an n-channel transistor for a generic 180-nm CMOS process

Parameter	**Value**
V_{DD}	1.8 V
C_{ox}	8.443 $\frac{fF}{\mu m^2}$
W_{min}	200 nm
L_{min}	180 nm
ΔW	54 nm
ΔL	-76 nm
V_{T0}	0.455 V
n	1.27
$I_{spec\square}$	715 nA
L_{sat}	26 nm
λ	20 $\frac{V}{\mu m}$
K_F	8.1×10^{-24} J
ρ	5.794×10^{-2} $\frac{V \cdot m^2}{A \cdot s}$
C_J	1 $\frac{fF}{\mu m^2}$
C_{JSW}	0.2 $\frac{fF}{\mu m}$
C_{GSo}	0.366 $\frac{fF}{\mu m}$
C_{GDo}	0.366 $\frac{fF}{\mu m}$
C_{GBo}	0 $\frac{fF}{\mu m}$

Note that the effective channel width and length are defined as follows

$$W_{eff} \triangleq W + \Delta W, \tag{1}$$

$$L_{eff} \triangleq L + \Delta L, \tag{2}$$

where W and L are drawn width and length.

Problem 1 Imposing the gain bandwidth product (unity gain frequency)

Design the CS amplifier shown in Fig. 1, for the following specifications at room temperature ($U_T = 25.9\,\text{mV}$):

$$f_u = 100\,MHz, \quad C_L = 1\,pF, \quad IC = 1, \quad L_{long} = 1\,\mu m, \quad L_{short} = 180\,nm.$$

Carry out the design procedure both for long- and short-channel devices in saturation, using the drawn lengths L_{long} and L_{short} respectively. Note that velocity saturation (VS) has to be accounted for in the short-channel case. We assume that the self-loading capacitance at the drain can be neglected (i.e. assume a constant load capacitance equal to C_L).

- Draw the equivalent small-signal schematic ignoring the transistor parasitic capacitances.
- Derive the transfer function $A_v(s) \triangleq \Delta V_{out}/\Delta V_{in}$ and extract the expressions of the dc gain, cut-off frequency and gain-bandwidth product (unity gain frequency) f_u.
- Find the transistor transconductance value G_m.
- Find the normalized source transconductance $g_{ms}(IC) \triangleq G_{ms}/G_{spec} = n\,G_m/G_{spec} = nU_T\,G_m/I_{spec}$ from the imposed inversion coefficient IC. Then, deduce the specific current I_{spec} and the bias current I_b. Calculate the power consumption.
- Find the W_{eff}/L_{eff} ratio and the effective width W_{eff} for both the long and short channel case using the given drawn length L. Derive the drawn width W.
- Deduce the output conductance value G_{ds} and then calculate the dc gain value assuming the bias current source is ideal.
- Simulate the circuit using the Smash simulator and compare the theoretical results with the simulations.

Problem 2 Imposing the power consumption

Design the same CS amplifier shown in Fig. 1 for the following specifications at room temperature ($U_T = 25.83\,\text{mV}$):

$$P_{max} = 100\,\mu W, \quad C_L = 1\,pF, \quad IC = 1, \quad L_{long} = 1\,\mu m, \quad L_{short} = 180\,nm.$$

Carry out the design procedure both for long- and short-channel devices in saturation, using the drawn lengths L_{long} and L_{short} respectively. Note that velocity saturation (VS) has to be accounted for in the short-channel case. We assume that the self-loading capacitance at the drain can be neglected (i.e. assume a constant load capacitance C_L).

- Find the bias current I_b for the specified maximum power consumption.
- Find the transconductance value of the transistor for the given inversion coefficient IC by means of the current efficiency.
- Find the unity gain-bandwidth product using the specific current I_{spec}. Calculate the power consumption.
- Find the W_{eff}/L_{eff} ratio and the effective width W_{eff} for both the long and short channel case using the given drawn length L. Derive the drawn width W.
- Deduce the output conductance value G_{ds} and then calculate the dc gain value assuming the bias current source is ideal.
- Simulate the circuit using the Smash simulator and compare the theoretical results with the simulations.

Problem 3 Imposing the gain bandwidth product and the current budget

Design the same CS amplifier shown in Fig. 1 imposing both the gain-bandwidth product and the current budget with the following specifications at room temperature ($U_T = 25.83\,\text{mV}$):

$$f_u = 9\,MHz, \quad I_b = 400\,nA, \quad C_L = 1\,pF, \quad L_{long} = 1\,\mu m.$$

Carry out the design procedure only for the long-channel case with $L = L_{long}$.

- Find the transistor transconductance value.
- Find the inversion coefficient IC by means of the current efficiency and then the I_{spec}.
- Find the W_{eff}/L_{eff} ratio and the effective width W_{eff} for the long channel case only using the given drawn length L. Derive the drawn width W.
- Deduce the output conductance value G_{ds} and then calculate the dc gain value assuming the bias current source is ideal.
- Simulate the circuit using the Smash simulator and compare the theoretical results with the simulations.

Problem 4 Imposing the input-referred noise

In this problem we want to design the CS amplifier shown in Fig. 1 imposing the input-referred noise including both the thermal and flicker noise. The specifications at room temperature ($U_T = 25.83\,\text{mV}$) are given below:

$$f_k = 100\,kHz, \quad \sqrt{S_{nth}} = 30\,nV/\sqrt{Hz}, \quad C_L = 1\,pF, \quad IC = 1, \quad \gamma_n = 0.72$$

where f_k is the noise corner frequency and S_{nth} is the input-referred thermal noise power spectral density (PSD).

- Using S_{nth} determine the transconductance G_m.
- Find the normalized transconductance $g_{ms}(IC)$.
- Determine the specific current I_{spec}, the bias current I_b and the W_{eff}/L_{eff} ratio.
- Using the noise corner frequency f_k, determine the effective gate area $W_{eff} \cdot L_{eff}$.
- Finally, calculate the effective and drawn dimensions of the transistor.
- Simulate the circuit using the Smash simulator and compare the theoretical results with the simulations.

Problem 5 Minimum current for a given gain-bandwidth product accounting for self-loading

In this problem we want to account for the self-loading effect which is particularly important when the transistor is getting wide which typically happens in weak inversion. The specifications at room temperature ($U_T = 25.83\,\text{mV}$) are given below:

$$f_u = 25\,MHz, \quad C_{L0} = 20\,fF, \quad C_W = 1.167\,\frac{fF}{\mu m}, \quad L = 1\,\mu m.$$

Follow the procedure illustrated in the lecture notes.

Problem 6 Minimum current for a given gain-bandwidth product accounting for self-loading

In this problem we want to account for the self-loading effect but use the additional degree of freedom, namely the transistor gate length, to set the dc gain. The specifications at room temperature ($U_T = 25.83\,\text{mV}$) are given below:

$$f_u = 25\,MHz, \quad A_{dc} = 40\,dB, \quad C_{L0} = 20\,fF, \quad C_W = 1.167\,\frac{fF}{\mu m}.$$

Follow the procedure illustrated in the lecture notes.