# Fundamentals of Analog & Mixed Signal VLSI Design
# Exercise 4 (9.10.2024)

Christian Enz

Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland

## Problem 1 Differential Pair with Resistive Load

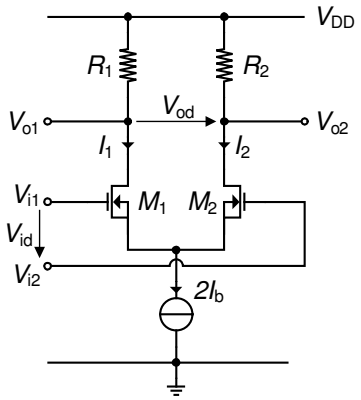


Figure 1: Differential pair.

Fig. 1 shows a differential pair composed of two NMOS transistors $M_1$ and $M_2$, loaded with resistors $R_1$ and $R_2$, respectively. Since there are two input terminals, the output current or voltage depends on both the input voltages $V_{i1}$ and $V_{i2}$. It is usually more interesting to express the output current or voltage in terms of the differential and common mode voltages $V_{id}$ and $V_{ic}$ defined as

$$V_{id} \triangleq V_{i1} - V_{i2} \tag{1a}$$

$$V_{ic} \triangleq \frac{V_{i1} + V_{i2}}{2}. \tag{1b}$$

The differential mode and common mode operations are defined for $V_{ic} = const.$ and for $V_{id} = 0$, respectively. The input terminals are set to an appropriate common mode voltage $V_{ic}$, to which a differential voltage $V_{id}$ is superimposed according to

$$V_{i1} = V_{ic} + \frac{V_{id}}{2} \tag{2a}$$

$$V_{i2} = V_{ic} - \frac{V_{id}}{2}. \tag{2b}$$

### 1.1 Small-signal analysis

- Draw the small-signal equivalent schematic of the circuit assuming the transistors are biased in saturation.
- Calculate the differential voltage gain
$$A_{vd} \triangleq \frac{V_{od}}{V_{id}}.$$
- Calculate the common-mode input voltage to differential output voltage gain
$$A_{vc} \triangleq \frac{V_{od}}{V_{ic}}.$$

## 1.2 Noise analysis

- Draw the small-signal equivalent schematic of the circuit assuming the transistors are biased in saturation and including all the noise sources.
- Calculate the output noise power spectral density (PSD) or output noise resistance assuming that the transistors and resistors are perfectly matched.
- Calculate the input-referred thermal noise PSD and the equivalent thermal noise resistance $R_{nin,th}$.
- Calculate the input-referred flicker noise PSD and the equivalent flicker noise resistance $R_{nin,fl}$.
- Calculate the total output thermal noise power assuming that there is an output capacitance $C$ in parallel with each of the load resistance $R_1$ and $R_2$ (assume that transistors, resistors and capacitors are perfectly matched).

## 1.3 Offset analysis

Mismatch between the two transistors of the differential pair $M_1$-$M_2$ and of the resistors $R_1$-$R_2$ cause some non-zero differential output voltage even for a zero differential input voltage $V_{id} = 0$.

- Calculate the differential mode output mismatch voltage in terms of drain current mismatch $\Delta I_D$ and resistance mismatch $\Delta R$. Hint: use the above noise analysis where the noise currents are replaced by current mismatch.
- Calculate the input-referred offset voltage in terms of resistor mismatch $\Delta R$ and MOS transistor mismatch ($\beta$ and $V_{T0}$ mismatch).
- Determine the variance of the input referred offset voltage. How can it be minimized?

## 1.4 Common-mode input range analysis (CMIR) and differential-mode output range analysis (DMOR)

- Calculate the minimum and maximum common-mode input voltages $V_{ic,min}$ and $V_{ic,max}$. For this analysis, $V_{id}$ is set to 0 and the ideal current source is replaced by a transistor ($M_2$).
- Calculate the minimum and maximum output voltages $V_{o,min}$ and $V_{o,max}$; deduce the differential output voltage $\Delta V_{od,max}$.

## 1.5 Design

Design the differential pair, i.e. size the transistors, determine the values of the resistors and the bias current, to meet the following specifications:

$$A_0 = 25\,dB, \quad R_{in,th} = 10\,k\Omega, \quad \sigma_{Vos} = 2\,mV.$$

Assume that each transistor is biased at the edge of weak inversion with $IC = 0.1$. Use a generic 180 nm CMOS process with the following parameters:

$$I_{spec\square} = 715\,nA, \quad V_{T0} = 0.455\,V, \quad n = 1.27, \quad \rho_n = 58 \times 10^{-3}\,\frac{V\,m^2}{A\,s}.$$

- Carry out the design assuming that the circuit is biased with $V_{DD} = 1.8\,V$ and that $V_{ic}$ is set to $0.8\,V$.
- What happens if $V_{DD} = 1\,V$? Can you use the same design as before and fulfill all the specifications? Using the same $V_{ic}$, get the new $\Delta V_{od,max}$ and propose an alternative design relaxing one of the specifications.

# Solutions to Exercise 4 (9.10.2024)

## Problem 1 Differential Pair with Resistive Load

### 1.1 Small-signal analysis

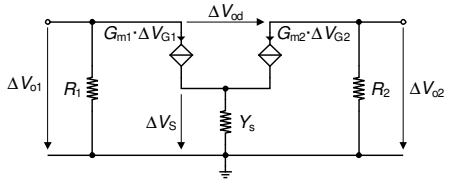


Figure 2: Small-signal equivalent circuit of Fig. 1.

Fig. 2 shows the small-signal schematic of the differential pair of Fig. 1 where $Y_s$ corresponds to the admittance to ground at the common source node made of the output conductance of the bottom current source and the total capacitance between the common source node and ground.

If the transistors and resistances are perfectly matched, in small-signal operation (i.e. $G_{m1} = G_{m2} = G_m$ and $R_1 = R_2 = R$), an increase of the gate voltage of $M_1$ by $\Delta V_{id}/2$ combined with a decrease of the gate voltage of $M_2$ by the same amount keeps the common source node unchanged. This node can therefore be considered as a virtual AC ground. The circuit then reduces to a common-source stage loaded by a resistance $R$ which has a voltage gain $-G_m R$. The differential stage has therefore the same ideal voltage gain $A_{vd} = -G_m R$ as the common-source stage.

Of course we can find this results by solving the KCL of the equivalent small-signal circuit of Fig. 2. Writing the KCL for the three nodes leads to

$$G_{m1}\,\Delta V_{G1} + \Delta V_{o1}/R_1 = 0, \tag{3a}$$
$$G_{m2}\,\Delta V_{G2} + \Delta V_{o2}/R_2 = 0, \tag{3b}$$
$$G_{m1}\,\Delta V_{G1} + G_{m2}\,\Delta V_{G2} = Y_s\,\Delta V_S. \tag{3c}$$

Additionally, the incremental gate voltages are related to the input voltages according to

$$\Delta V_{G1} = \Delta V_{i1} - \Delta V_S, \tag{4a}$$
$$\Delta V_{G2} = \Delta V_{i2} - \Delta V_S. \tag{4b}$$

Solving (3) and (4) together, we obtain the incremental output voltages as

$$\Delta V_{o1} = -G_{m1}\,R_1 \cdot \frac{(G_{m2} + Y_s)\,\Delta V_{i1} - G_{m2}\Delta V_{i2}}{G_{m1} + G_{m2} + Y_s}, \tag{5a}$$
$$\Delta V_{o2} = -G_{m2}\,R_2 \cdot \frac{-G_{m1}\Delta V_{i1} + (G_{m1} + Y_s)\Delta V_{i2}}{G_{m1} + G_{m2} + Y_s}. \tag{5b}$$

We now express the output voltages in terms of the differential and common mode voltages $\Delta V_{id}$ and $\Delta V_{ic}$ defined as

$$\Delta V_{id} \triangleq \Delta V_{i1} - \Delta V_{i2}, \tag{6a}$$
$$\Delta V_{ic} \triangleq \frac{\Delta V_{i1} + \Delta V_{i2}}{2}, \tag{6b}$$

such that

$$\Delta V_{i1} = \Delta V_{ic} + \frac{\Delta V_{id}}{2}, \tag{7a}$$
$$\Delta V_{i2} = \Delta V_{ic} - \frac{\Delta V_{id}}{2}. \tag{7b}$$

The differential mode of operation is then defined for $\Delta V_{ic} = 0$, whereas the common mode operation corresponds to $\Delta V_{id} = 0$.

The *differential voltage gain*, is then defined as

$$A_{vd} \triangleq \frac{\Delta V_{od}}{\Delta V_{id}} = \frac{\Delta V_{o1} - \Delta V_{o2}}{\Delta V_{id}} \tag{8}$$

and is obtained from (5) as

$$A_{vd} = -\frac{G_{m1}\, G_{m2}\,(R_1 + R_2) + (G_{m1} R_1 + G_{m2} R_2)\, Y_s/2}{G_{m1} + G_{m2} + Y_s}. \tag{9}$$

Assuming that the transistors and resistances are perfectly matched $G_{m1} = G_{m2} = G_m$ and $R_1 = R_2 = R$, the expression for the differential voltage gain simplifies to the expected result

$$A_{vd} = -G_m\, R. \tag{10}$$

One of the main feature of the differential pair is to reject the input common-mode voltage. In the case the transistors and resistances are perfectly matched, the common-mode to differential output voltage gain is ideally equal to zero because $\Delta V_{o1} = \Delta V_{o2}$. However, if there is a mismatch between the transistors or the resistances, $\Delta V_{o1} \neq \Delta V_{o2}$ and therefore a differential output voltage is generated. The common-mode to differential voltage gain is given by

$$A_{vc} = Y_s \cdot \frac{G_{m2}\, R_2 - G_{m1}\, R_1}{G_{m1} + G_{m2} + Y_s} \tag{11}$$

From (11), we see that for a perfect matching $A_{vc} = 0$ since $G_{m1}\, R_1 = G_{m2}\, R_2 = G_m\, R$. Note that at low frequency, $Y_s$ is equal to the output conductance $G_{ds}$ of the bottom current source. The common-mode to differential voltage gain is proportional to $G_{ds}$. We can account for the mismatch by replacing

$$G_{m1} = G_m + \frac{\Delta G_m}{2}, \tag{12a}$$

$$G_{m2} = G_m - \frac{\Delta G_m}{2}, \tag{12b}$$

$$R_1 = R + \frac{\Delta R}{2}, \tag{12c}$$

$$R_2 = R - \frac{\Delta R}{2}, \tag{12d}$$

resulting in

$$A_{vc} = -G_{ds} \cdot \frac{G_m\, R}{G_{ds} + 2G_m} \cdot \left(\frac{\Delta G_m}{G_m} + \frac{\Delta R}{R}\right) \cong -\frac{G_{ds}\, R}{2}\left(\frac{\Delta G_m}{G_m} + \frac{\Delta R}{R}\right), \tag{13}$$

since $G_m \gg G_{ds}$.

The ability of the differential pair to reject the differential voltage is measured by the common-mode rejection ratio or CMRR defined as

$$CMRR \triangleq \frac{|A_{vd}|}{|A_{vc}|} \cong \frac{2G_m/G_{ds}}{\frac{\Delta G_m}{G_m} + \frac{\Delta R}{R}}. \tag{14}$$

From (14), we observe that the *CMRR* is proportional to the transistor intrinsic gain (or self-gain) $G_m/G_{ds}$.

## 1.2 Noise analysis

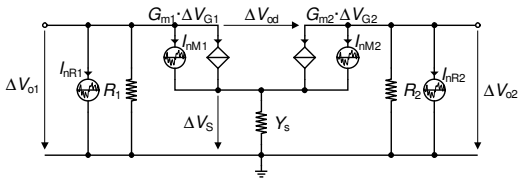


Figure 3: Small-signal equivalent circuit of Fig. 1 including the noise sources.

The equivalent small-signal circuit of Fig. 1 including all the noise sources is shown in Fig. 3. For noise analysis the inputs are connected to the dc common-mode input voltage $V_{ic}$ so that $\Delta V_{i1} = \Delta V_{i2} = 0$ and $\Delta V_{G1} = \Delta V_{G2} = -\Delta V_S$. The output noise voltages are then simply given by

$$\Delta V_{no1} = -R \cdot (I_{nM1} + I_{nR1}), \tag{15a}$$

$$\Delta V_{no2} = -R \cdot (I_{nM2} + I_{nR2}). \tag{15b}$$

and the differential output noise voltage is given by

$$\Delta V_{nout} = -R \cdot (I_{nM1} + I_{nR1} - I_{nM2} - I_{nR2}). \tag{16}$$

The PSD of the differential output noise voltage is then simply given by

$$S_{nout} = R^2 \cdot (S_{I_{nM1}} + S_{I_{nR1}} + S_{I_{nM2}} + S_{I_{nR2}}) = 2R^2 \cdot (S_{I_{nM}} + S_{I_{nR}}). \tag{17}$$

which can also be written in terms of the output noise resistance $R_{nout}$

$$S_{nout} = 4k_B T\, R_{nout} \tag{18}$$

with

$$R_{nout} = R^2 \cdot 2(G_{nM} + G_{nR}). \tag{19}$$

The noise conductances $G_{nM}$ and $G_{nR}$ are given by

$$G_{nM} = \gamma_n\, G_m + \frac{\rho_n}{W\, L\, f}, \tag{20a}$$

$$G_{nR} = \frac{1}{R}. \tag{20b}$$

The input-referred noise resistance at low-frequency is then given by

$$R_{nin} = \frac{R_{nout}}{|A_{vd}|^2} = \frac{R_{nout}}{(G_m\, R)^2} = 2\frac{G_{nM} + G_{nR}}{G_m^2}. \tag{21}$$

The input-referred thermal noise resistance is then given by

$$R_{nin,th} = \frac{2\gamma_n}{G_m} \cdot (1 + \eta_{th}), \tag{22}$$

where $\eta_{th}$ represents the contribution of the resistances normalized to the contribution of the differential pair

$$\eta_{th} = \frac{1}{\gamma_n\, G_m\, R}. \tag{23}$$

From (23), we see that the larger the differential gain, the lower the contribution of the resistances to the input-referred thermal noise resistance, which is consistent with the intuition that the larger the gain of the first stage the lower the contribution of the following stages to the input-referred noise.

The input-referred flicker noise resistance is only due to the transistor since the resistances only generate thermal noise

$$R_{nin,fl}(f) = 2\frac{\rho_n}{W\, L\, f}. \tag{24}$$

If we include a capacitance $C$ in parallel to the resistors $R$, the output thermal noise PSD is given by

$$S_{nout,th} = \frac{S_0}{1 + (\omega/\omega_c)^2}, \tag{25}$$

with

$$S_0 = 8k_B T \cdot R \cdot (\gamma_n\, G_m\, R + 1) \tag{26}$$

and $\omega_c = 1/(RC)$ is the cut-off frequency. The output noise is therefore a $1^{\text{st}}$-order low-pass filtered white noise. The noise bandwidth is therefore given by

$$B_n = \frac{\omega_c}{4} = \frac{1}{4RC}, \tag{27}$$

The resulting output thermal noise power is then given by

$$V_{nout,th}^2 = \frac{2k_B T}{C} \cdot (\gamma_n\, G_m\, R + 1) = \frac{2k_B T\, \gamma_n\, G_m\, R}{C} + \frac{2k_B T}{C} \cong \frac{2k_B T}{C} \cdot \gamma_n\, G_m\, R \tag{28}$$

assuming that $G_m\, R \gg 1$. We see that the contribution of the resistance is simply $2k_B T/C$ because the noise level is proportional to $R$ while the cut-off frequency is inversely proportional to $R$. The contribution of the differential pair depends on $G_m$ because $G_m$ sets the noise level but the cut-off frequency is set by $R$ and does not depend on $G_m$.

## 1.3 Offset analysis

Because of the transistor and resistor mismatch, the output voltage is not equal to zero when the differential input voltage is zero. To calculate the offset voltage we can reuse the expression of the output noise voltage (15) obtained in the noise analysis and replace

$$I_{nM1} = +\frac{\Delta I_D}{2}, \tag{29a}$$

$$I_{nM2} = -\frac{\Delta I_D}{2}, \tag{29b}$$

$$I_{nR1} = +\frac{I_b}{R} \cdot \frac{\Delta R}{2}, \tag{29c}$$

$$I_{nR2} = -\frac{I_b}{R} \cdot \frac{\Delta R}{2}. \tag{29d}$$

The resulting differential output offset voltage is given by

$$V_{os,out} = -R\, I_b \cdot \left( \frac{\Delta R}{R} + \frac{\Delta I_D}{I_b} \right) \tag{30}$$

The dc input-referred offset voltage is then given by

$$V_{os} = \frac{V_{os,out}}{-G_m R} = \frac{I_b}{G_m} \cdot \left( \frac{\Delta R}{R} + \frac{\Delta I_D}{I_b} \right). \tag{31}$$

The variance of the input-referred offset voltage is then given by

$$\sigma^2_{V_{os}} = \left( \frac{I_b}{G_m} \right)^2 \cdot (\sigma^2_{\Delta R/R} + \sigma^2_{\Delta I_D/I_D}). \tag{32}$$

The variance $\sigma^2_{\Delta I_D/I_D}$ is given by

$$\sigma^2_{\Delta I_D/I_D} = \sigma^2_{\Delta\beta/\beta} + \left( \frac{G_m}{I_b} \right)^2 \cdot \sigma^2_{\Delta V_{T0}}, \tag{33}$$

resulting in

$$\sigma^2_{V_{os}} = \sigma^2_{\Delta V_{T0}} + \left( \frac{I_b}{G_m} \right)^2 \cdot \left( \sigma^2_{\Delta R/R} + \sigma^2_{\Delta\beta/\beta} \right) \tag{34}$$

The variances $\sigma^2_{\Delta V_{T0}}$ and $\sigma^2_{\Delta\beta/\beta}$ can be expressed in terms of the transistor area according to

$$\sigma^2_{\Delta V_{T0}} = \frac{A^2_{\Delta V_{T0}}}{W\, L}, \tag{35a}$$

$$\sigma^2_{\Delta\beta/\beta} = \frac{A^2_{\beta}}{W\, L}. \tag{35b}$$

From (34), we see that the contributions of the resistance mismatch and transistor $\beta$ mismatch to the input-referred offset voltage can be minimized by biasing the differential pair in weak inversion. The input-referred offset reduces then to the transistor $V_{T0}$ mismatch.