

Fundamentals of Analog & Mixed Signal VLSI Design

Exercise 4 (9.10.2024)

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Problem 1 Differential Pair with Resistive Load

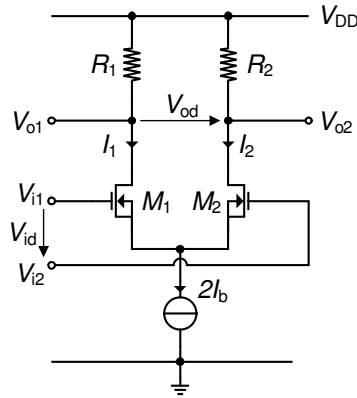


Figure 1: Differential pair.

Fig. 1 shows a differential pair composed of two NMOS transistors M_1 and M_2 , loaded with resistors R_1 and R_2 , respectively. Since there are two input terminals, the output current or voltage depends on both the input voltages V_{i1} and V_{i2} . It is usually more interesting to express the output current or voltage in terms of the differential and common mode voltages V_{id} and V_{ic} defined as

$$V_{id} \triangleq V_{i1} - V_{i2} \quad (1a)$$

$$V_{ic} \triangleq \frac{V_{i1} + V_{i2}}{2}. \quad (1b)$$

The differential mode and common mode operations are defined for $V_{ic} = \text{const.}$ and for $V_{id} = 0$, respectively. The input terminals are set to an appropriate common mode voltage V_{ic} , to which a differential voltage V_{id} is superimposed according to

$$V_{i1} = V_{ic} + \frac{V_{id}}{2} \quad (2a)$$

$$V_{i2} = V_{ic} - \frac{V_{id}}{2}. \quad (2b)$$

1.1 Small-signal analysis

- Draw the small-signal equivalent schematic of the circuit assuming the transistors are biased in saturation.
- Calculate the differential voltage gain

$$A_{vd} \triangleq \frac{V_{od}}{V_{id}}.$$

- Calculate the common-mode input voltage to differential output voltage gain

$$A_{vc} \triangleq \frac{V_{od}}{V_{ic}}.$$

1.2 Noise analysis

- Draw the small-signal equivalent schematic of the circuit assuming the transistors are biased in saturation and including all the noise sources.
- Calculate the output noise power spectral density (PSD) or output noise resistance assuming that the transistors and resistors are perfectly matched.
- Calculate the input-referred thermal noise PSD and the equivalent thermal noise resistance $R_{in,th}$.
- Calculate the input-referred flicker noise PSD and the equivalent flicker noise resistance $R_{in,fl}$.
- Calculate the total output thermal noise power assuming that there is an output capacitance C in parallel with each of the load resistance R_1 and R_2 (assume that transistors, resistors and capacitors are perfectly matched).

1.3 Offset analysis

Mismatch between the two transistors of the differential pair M_1 - M_2 and of the resistors R_1 - R_2 cause some non-zero differential output voltage even for a zero differential input voltage $V_{id} = 0$.

- Calculate the differential mode output mismatch voltage in terms of drain current mismatch ΔI_D and resistance mismatch ΔR . Hint: use the above noise analysis where the noise currents are replaced by current mismatch.
- Calculate the input-referred offset voltage in terms of resistor mismatch ΔR and MOS transistor mismatch (β and V_{T0} mismatch).
- Determine the variance of the input referred offset voltage. How can it be minimized?

1.4 Common-mode input range analysis (CMIR) and differential-mode output range analysis (DMOR)

- Calculate the minimum and maximum common-mode input voltages $V_{ic,min}$ and $V_{ic,max}$. For this analysis, V_{id} is set to 0 and the ideal current source is replaced by a transistor (M_2).
- Calculate the minimum and maximum output voltages $V_{o,min}$ and $V_{o,max}$; deduce the differential output voltage $\Delta V_{od,max}$.

1.5 Design

Design the differential pair, i.e. size the transistors, determine the values of the resistors and the bias current, to meet the following specifications:

$$A_0 = 25 \text{ dB}, \quad R_{in,th} = 10 \text{ k}\Omega, \quad \sigma_{V_{os}} = 2 \text{ mV}.$$

Assume that each transistor is biased at the edge of weak inversion with $IC = 0.1$. Use a generic 180 nm CMOS process with the following parameters:

$$I_{spec\Box} = 715 \text{ nA}, \quad V_{T0} = 0.455 \text{ V}, \quad n = 1.27, \quad \rho_n = 58 \times 10^{-3} \frac{\text{V m}^2}{\text{A s}}.$$

- Carry out the design assuming that the circuit is biased with $V_{DD} = 1.8 \text{ V}$ and that V_{ic} is set to 0.8 V .
- What happens if $V_{DD} = 1 \text{ V}$? Can you use the same design as before and fulfill all the specifications? Using the same V_{ic} , get the new $\Delta V_{od,max}$ and propose an alternative design relaxing one of the specifications.