Fundamentals of Analog & Mixed Signal VLSI Design
Exercise 2 (25.09.2024)

Christian Enz

Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland

Problem 1 The differential pair

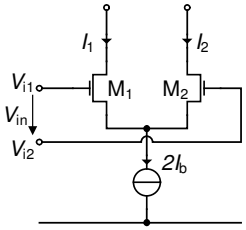

Figure 1: The differential pair.

Fig. 1 shows the schematic of the basic differential pair. The differential input voltage is defined as $V_{id} \triangleq V_{i1} - V_{i2}$, whereas the differential output current is defined as $I_{od} \triangleq I_1 - I_2$.

1.1 Both transistors in weak inversion

1.1.1 Large-signal differential transfer characteristic

Derive the large-signal expression of the differential output current I_{od} as a function of the differential input voltage V_{id} assuming that both transistors are biased in weak inversion and saturation.

1.1.2 Small-signal transconductance

Derive the small-signal transconductance from the large-signal transfer function obtained above and its particular value G_{m0} at $V_{id} = 0$. What is the approximate linear range if the differential pair is modeled by a piece-wise linear characteristic having a slope G_{m0} equal to that of the differential pair at $V_{id} = 0$?

1.2 Both transistors in strong inversion

1.2.1 Large-signal differential transfer characteristic

Derive the large-signal expression of the differential output current I_{od} as a function of the differential input voltage V_{id} assuming that both transistors are biased in strong inversion and saturation.

1.2.2 Small-signal transconductance

Derive the small-signal transconductance from the large-signal transfer function obtained above and its particular value G_{m0} at $V_{id} = 0$. What is the approximate linear range if the differential pair is modeled by a piece-wise linear characteristic having a slope G_{m0} equal to that of the differential pair at $V_{id} = 0$?

1.3 Optional: Both transistors in any modes of operation (saturation)

We can use the EKV charge-based model to derive an expression of the differential input voltage as a function of the differential output current valid in any modes of operation (in saturation). In order to do this, first express the input voltages V_{i1} and V_{i2} normalized to $2nU_T$ as a function of the normalized source charges q_{s1} and q_{s2}. Then find an expression of i_1 and i_2 defined as

$$i_1 \triangleq \frac{I_1}{2I_b} = \frac{i_{d1}}{2IC_q}, \tag{1a}$$

$$i_2 \triangleq \frac{I_2}{2I_b} = \frac{i_{d2}}{2IC_q}, \tag{1b}$$

with $i_{d1} \triangleq I_1/I_{spec}$, $i_{d2} \triangleq I_2/I_{spec}$ and $IC_q \triangleq I_b/I_{spec}$ and where I_{spec} is the specific current of M_1 and M_2 and IC_q is the inversion coefficient of M_1 and M_2 at the quiescent point, i.e. for $V_{id} = 0$. You can then invert i_1 and i_2 to obtain expressions of q_{s1} and q_{s2} in terms of $i_{od} \triangleq i_1 - i_2$ and parameter IC_q. Sweeping the normalized output current i_{od} for a given IC_q, you get the corresponding differential input voltage v_{id}.

Problem 2 The inverter as a transconductance amplifier

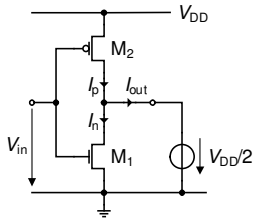

Figure 2: The inverter used as a transconductance amplifier.

As shown in Fig. 2, the inverter can be used as a class AB transconductance amplifier. Derive the large-signal output current $I_{out} = I_p - I_n$ versus the input voltage V_{in} assuming that both transistors are biased in weak inversion and saturation and have the same slope factor $n_n = n_p = n$. Note that the output voltage is maintained constant at $V_{DD}/2$ to calculate the output current I_{out}. What is limiting the output current?

Problem 3 Effect of velocity saturation on the gate transconductance

An nMOS transistor is biased with a current of $I_b = 20\,\mu A$ at an inversion coefficient $IC = 30$ to drive a large load capacitance $C_L = 5\,pF$. Calculate its gate transconductance G_m and bandwidth assuming its slope factor is $n = 1.3$ and $U_T = 26\,mV$ in the following cases.

3.1 Long-channel case

Assume the channel is long enough to ignore the effect of velocity saturation.

3.2 Short-channel case

Assume the transistor length is short resulting in a velocity saturation parameter $\lambda_c = 1/3$. How much smaller is the gate transconductance and bandwidth with velocity saturation compared to the long-channel case?

Solutions to Exercise 2 (25.09.2024)

Problem 1 The differential pair

1.1 Both transistors in weak inversion

1.1.1 Large-signal differential transfer characteristic

In the follwoing analysis it is assumed that M_1 and M_2 are perfectly matched, leading to

$$V_{T01} = V_{T02} = V_{T0}, \tag{2a}$$
$$I_{D01} = I_{D02} = I_{D0}, \tag{2b}$$
$$n_1 = n_2 = n. \tag{2c}$$

In the case both transistors are biased in weak inversion and saturation and since the bulks of M_1 and M_2 are connected to the ground, the drain currents are then given by

$$I_1 = I_{D0} \cdot \mathrm{e}^{\frac{V_{i1} - n\,V_S}{nU_T}}, \tag{3a}$$
$$I_2 = I_{D0} \cdot \mathrm{e}^{\frac{V_{i2} - n\,V_S}{nU_T}}, \tag{3b}$$

where V_S is the common source voltage of M_1 and M_2. The differential output current is then given by

$$I_{od} \triangleq I_1 - I_2 = I_{D0} \cdot \mathrm{e}^{\frac{-V_S}{U_T}} \cdot \left[\mathrm{e}^{\frac{V_{i1}}{nU_T}} - \mathrm{e}^{\frac{V_{i2}}{nU_T}}\right]. \tag{4}$$

Now, the sum of I_1 and I_2 is set by the bottom current source

$$I_1 + I_2 = 2I_b, \tag{5}$$

leading to

$$2I_b = I_{D0} \cdot \mathrm{e}^{\frac{-V_S}{U_T}} \cdot \left[\mathrm{e}^{\frac{V_{i1}}{nU_T}} + \mathrm{e}^{\frac{V_{i2}}{nU_T}}\right] \tag{6}$$

from which we get

$$I_{D0} \cdot \mathrm{e}^{\frac{-V_S}{U_T}} = \frac{2I_b}{\mathrm{e}^{\frac{V_{i1}}{nU_T}} + \mathrm{e}^{\frac{V_{i2}}{nU_T}}}. \tag{7}$$

Replacing (7) in (4) results in

$$I_{od} = 2I_b \cdot \frac{\mathrm{e}^{\frac{V_{i1}}{nU_T}} - \mathrm{e}^{\frac{V_{i2}}{nU_T}}}{\mathrm{e}^{\frac{V_{i1}}{nU_T}} + \mathrm{e}^{\frac{V_{i2}}{nU_T}}}. \tag{8}$$

The input voltages can be written in terms of differential and common mode voltages according to

$$V_{i1} = V_{ic} + \frac{V_{id}}{2}, \tag{9a}$$
$$V_{i2} = V_{ic} - \frac{V_{id}}{2}. \tag{9b}$$

Replacing in (8) results in

$$I_{od} = 2I_b \cdot \frac{\mathrm{e}^{\frac{V_{id}}{2nU_T}} - \mathrm{e}^{\frac{-V_{id}}{2nU_T}}}{\mathrm{e}^{\frac{V_{id}}{2nU_T}} + \mathrm{e}^{\frac{-V_{id}}{2nU_T}}} = 2I_b \cdot \tanh\left(\frac{V_{id}}{2nU_T}\right). \tag{10}$$

The differential output current I_{od} normalized to $2I_b$ can then be written as

$$i_{od} \triangleq \frac{I_{od}}{2I_b} = \tanh(v_{id}), \tag{11}$$

where $v_{id} \triangleq V_{id}/(2nU_T)$.

1.1.2 Small-signal transconductance

The small-signal transconductance is defined by

$$G_m \triangleq \frac{\mathrm{d}I_{od}}{\mathrm{d}V_{id}} = G_{m0} \cdot \left[1 - \tanh^2\left(\frac{V_{id}}{2nU_T}\right)\right] \tag{12}$$

where G_{m0} is the transconductance for $V_{id} = 0$

$$G_{m0} = \frac{I_b}{nU_T}. \tag{13}$$

The small-signal transconductance normalized to G_{m0} is then given by

$$g_m \triangleq \frac{G_m}{G_{m0}} = 1 - \tanh^2(v_{id}). \tag{14}$$

The normalized differential output current i_{od} and normalized transconductance g_m are plotted versus the normalized differential input voltage v_{id} in Fig. 1.

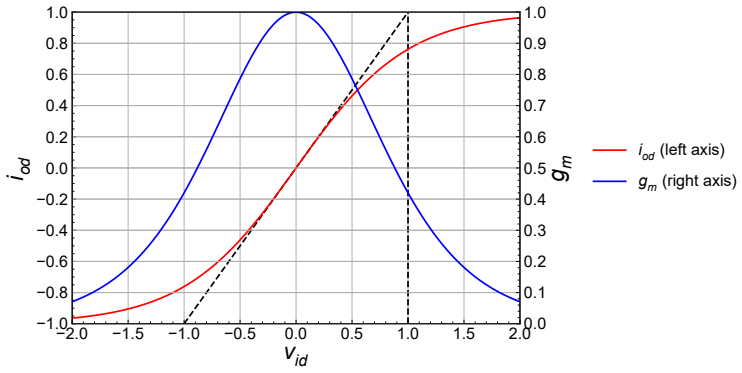

Figure 1: Differential current i_{od} and transconductance g_m versus differential input voltage v_{id} for both transistors M_1 and M_2 biased in weak inversion and saturation.

1.2 Both transistors in strong inversion

1.2.1 Large-signal differential transfer characteristic

We again will assume that the two transistors M_1 an M_2 are perfectly matched, which means that

$$V_{T01} = V_{T02} = V_{T0}, \tag{15a}$$
$$\beta_1 = \beta_2 = \beta, \tag{15b}$$
$$n_1 = n_2 = n. \tag{15c}$$

In the case both transistors are biased in strong inversion and saturation and since the bulks of M_1 and M_2 are connected to the ground, the drain currents are given by

$$I_1 = \frac{\beta}{2n} \cdot (V_{i1} - V_{T0} - n\,V_S)^2, \tag{16a}$$
$$I_2 = \frac{\beta}{2n} \cdot (V_{i2} - V_{T0} - n\,V_S)^2, \tag{16b}$$

where V_S is the voltage of the common source node. Solving the above equations together with

$$I_{od} = I_1 - I_2, \tag{17a}$$
$$I_1 + I_2 = 2I_b, \tag{17b}$$
$$V_{i1} = V_{ic} + \frac{V_{id}}{2}, \tag{17c}$$
$$V_{i2} = V_{ic} - \frac{V_{id}}{2}, \tag{17d}$$
$$V_{id} = V_{i1} - V_{i2}, \tag{17e}$$

leads to

$$I_{od} = V_{id} \cdot \sqrt{\frac{\beta}{2nI_b}} \cdot \sqrt{1 - \frac{\beta}{2nI_b} \cdot \left(\frac{V_{id}}{2}\right)^2} \tag{18}$$

valid for

$$|V_{id}| < 2\sqrt{\frac{2nI_b}{\beta}} = 2(V_{ic} - V_{T0} - V_S). \tag{19}$$

The differential output current I_{od} can be normalized to the maximum output current $2I_b$

$$i_{od} \triangleq \frac{I_{od}}{2I_b} = v_{id} \cdot \sqrt{1 - \left(\frac{v_{id}}{2}\right)^2}, \tag{20}$$

valid for

$$|v_{id}| < \sqrt{2}, \tag{21}$$

where

$$v_{id} \triangleq \frac{V_{id}}{\sqrt{2nI_b/\beta}} = \frac{V_{id}}{V_G - V_{T0} - n\,V_S}. \tag{22}$$

1.2.2 Small-signal transconductance

The small-signal transconductance is given by

$$G_m \triangleq \frac{\mathrm{d}I_{od}}{\mathrm{d}V_{id}} = G_{m0} \cdot \frac{2 - v_{id}^2}{\sqrt{4 - v_{id}^2}}, \tag{23}$$

where

$$G_{m0} = \sqrt{\frac{2\beta I_b}{n}} \tag{24}$$

is the transconductance for $V_{id} = 0$.

The normalized differential output current i_{od} and normalized transconductance g_m are plotted versus the normalized differential input voltage v_{id} in Fig. 2.

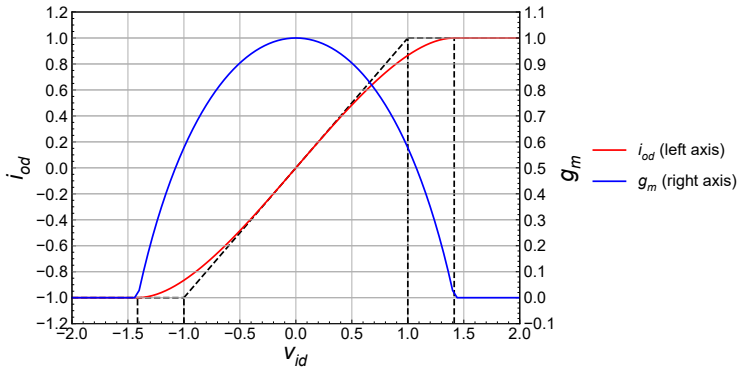

Figure 2: Differential current i_{od} and transconductance g_m versus differential input voltage v_{id} for both transistors M_1 and M_2 biased in strong inversion and saturation.

1.3 Both transistors in any modes of operation (saturation)

1.3.1 Large-signal differential transfer characteristic

We can use the EKV charge-based model to express the gate voltages of M_1 and M_2 in terms of q_{s1} and q_{s2} according to

$$\frac{V_{i1} - V_{T0} - n\,V_S}{nU_T} = 2q_{s1} + \ln(q_{s1}), \tag{25a}$$

$$\frac{V_{i2} - V_{T0} - n\,V_S}{nU_T} = 2q_{s2} + \ln(q_{s2}). \tag{25b}$$

If we want to be consistent with the analysis of the differential pair in weak inversion we need to use the same normalization. This means that the voltages need to be normalized to $2nU_T$, leading to

$$v_{i1} - v_{t0n} - v_s = q_{s1} + \tfrac{1}{2}\ln(q_{s1}), \tag{26a}$$

$$v_{i2} - v_{t0n} - v_s = q_{s2} + \tfrac{1}{2}\ln(q_{s2}), \tag{26b}$$

where

$$v_{i1} \triangleq \frac{V_{i1}}{2nU_T}, \tag{27a}$$

$$v_{i2} \triangleq \frac{V_{i2}}{2nU_T}, \tag{27b}$$

$$v_s \triangleq \frac{V_S}{2nU_T}. \tag{27c}$$

The normalized differential input voltage v_{id} is then given by subtracting (26b) to (26a) resulting in

$$v_{id} \triangleq \frac{V_{id}}{2nU_T} = v_{i1} - v_{i2} = q_{s1} - q_{s2} + \tfrac{1}{2}\ln\left(\frac{q_{s1}}{q_{s2}}\right) \tag{28}$$

We need to be careful with the normalization of the currents. In order to have the output differential current $I_{od} = I_1 - I_2$ normalized to the maximum output current $2I_b$, like it was done for the analysis in weak and strong inversion, we need to define the normalized currents i_1, i_2 and i_{od} as

$$i_1 \triangleq \frac{I_1}{2I_b}, \tag{29a}$$

$$i_2 \triangleq \frac{I_2}{2I_b}, \tag{29b}$$

$$i_{od} \triangleq \frac{I_{od}}{2I_b} = \frac{I_1 - I_2}{2I_b} = i_1 - i_2. \tag{29c}$$

The normalized source charges q_{s1} and q_{s2} are related to the normalized drain currents i_{d1} and i_{d2} according to

$$i_{d1} \triangleq \frac{I_1}{I_{spec}} = q_{s1} \cdot (q_{s1} + 1), \tag{30a}$$

$$i_{d2} \triangleq \frac{I_2}{I_{spec}} = q_{s2} \cdot (q_{s2} + 1). \tag{30b}$$

Notice that i_1 and i_2 are different than i_{d1} and i_{d2} since the former are normalized to $2I_b$, whereas the latter are normalized to I_{spec}. They are related according to

$$i_1 = \frac{i_{d1}}{2IC_q}, \tag{31a}$$

$$i_2 = \frac{i_{d2}}{2IC_q}, \tag{31b}$$

where

$$IC_q \triangleq \frac{I_b}{I_{spec}} \tag{32}$$

corresponds to the inversion coefficient of M_1 and M_2 at the quiescent operating point, i.e. for $V_{id} = 0$.

Solving the above set of equations for q_{s1} and q_{s2} results in

$$q_{s1} = \frac{\sqrt{4IC_q(1 + i_{od}) + 1} - 1}{2}, \tag{33a}$$

$$q_{s2} = \frac{\sqrt{4IC_q(1 - i_{od}) + 1} - 1}{2}. \tag{33b}$$

We can now sweep the normalized differential output current for a given IC_q and then calculate q_{s1} and q_{s2} according to (**??**) and use them to calculate v_{id} according to (28). The result is plotted in Fig. 3 for different IC_q.

We clearly see that increasing the inversion coefficient IC_q from weak inversion to strong inversion extends the linear range from $4nU_T$ to $2(V_{ic} - V_{T0} - nV_S)$ at the cost of a reduced transconductance efficiency G_{m0}/I_b.

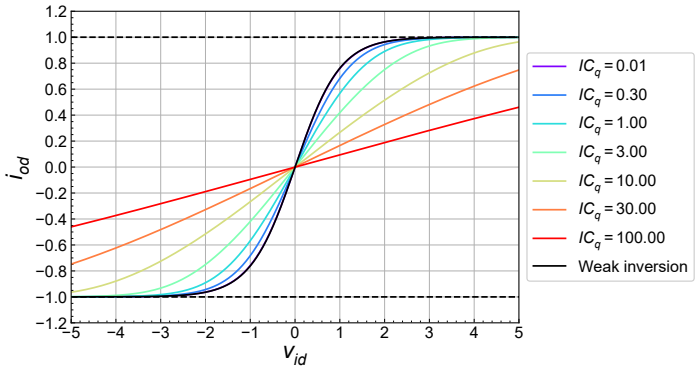

Figure 3: Differential current i_{od} versus differential input voltage v_{id} valid in all regions of operation (assuming M_1 and M_2 in saturation).

1.3.2 Small-signal transconductance

In the previous section we have derived an expression of V_{id} in terms of q_{s1} and q_{s2} which depend on I_{od}. We can derive the transconductance by differentiating V_{id} wrt I_{od}

$$\frac{\mathrm{d}V_{id}}{\mathrm{d}I_{od}} = \frac{1}{G_m} \tag{34}$$

or in normalized form

$$\frac{\mathrm{d}v_{id}}{\mathrm{d}i_{od}} \cdot \frac{2nU_T}{2I_b} = \frac{1}{G_m}. \tag{35}$$

The transconductance can then be written as

$$G_m \cdot \frac{nU_T}{I_b} = \left(\frac{\mathrm{d}v_{id}}{\mathrm{d}i_{od}}\right)^{-1} = \frac{\mathrm{d}i_{od}}{\mathrm{d}v_{id}} = g_m. \tag{36}$$

so that

$$g_m \triangleq \frac{\mathrm{d}i_{od}}{\mathrm{d}v_{id}} = \frac{G_m}{I_b/(nU_T)} \tag{37}$$

It can be shown that

$$g_m = \frac{4}{IC_q} \cdot \frac{q_{s1} \cdot q_{s2}}{q_{s1} + q_{s2}} \tag{38}$$

with q_{s1} and q_{s2} given by (33a) and (33b).

Now, we want to plot g_m normalized to its value at $v_{id} = 0$

$$g_{m0} \triangleq g_m(v_{id} = 0). \tag{39}$$

For $v_{id} = 0$, we have $i_{od} = 0$ and from (33), we get

$$q_s \triangleq = q_{s1}\big|_{v_{id}=0} = q_{s2}\big|_{v_{id}=0} = \frac{\sqrt{4IC_q + 1} - 1}{2}. \tag{40}$$

g_{m0} can therefore be written as

$$g_{m0} = \frac{q_s}{IC_q} = \frac{\sqrt{4IC_q + 1} - 1}{2IC_q}. \tag{41}$$

The transconductance normalized to the value it takes at $v_{id} = 0$ is therefore given by

$$\frac{G_m}{G_{m0}} = \frac{g_m}{g_{m0}} = \frac{2}{q_s} \cdot \frac{q_{s1} \cdot q_{s2}}{q_{s1} + q_{s2}} \tag{42}$$

with q_s, q_{s1} and q_{s2} given by (40), (33a) and (33b), respectively.

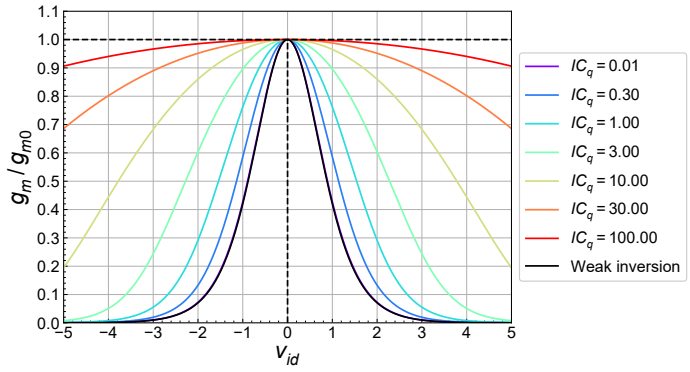

Figure 4: Transconductance normalized to its value at $v_{id} = 0$ versus differential input voltage v_{id} valid in all regions of operation (assuming M_1 and M_2 in saturation).

Problem 2 The inverter as a transconductance amplifier

Assuming both transistors are biased in weak inversion and saturation, the drain currents are then given by

$$I_n = I_{specn} \cdot \mathrm{e}^{\frac{V_{Gn}-V_{T0n}}{n_n U_T}} = I_{D0n} \cdot \mathrm{e}^{\frac{V_{Gn}}{n_n U_T}}, \tag{43a}$$

$$I_p = I_{specp} \cdot e^{\frac{V_{Gp}-V_{T0p}}{n_p U_T}} = I_{D0p} \cdot \mathrm{e}^{\frac{V_{Gp}}{n_p U_T}}, \tag{43b}$$

where

$$I_{specn} = I_{specn\square} \cdot W_n/L_n, \tag{44a}$$

$$I_{specp} = I_{specp\square} \cdot W_p/L_p, \tag{44b}$$

and

$$I_{D0n} = I_{specn} \cdot \mathrm{e}^{\frac{-V_{T0n}}{n_n U_T}}, \tag{45a}$$

$$I_{D0p} = I_{specp} \cdot \mathrm{e}^{\frac{-V_{T0p}}{n_p U_T}}. \tag{45b}$$

The gate voltages are given by

$$V_{Gn} = V_{in} - V_{inq}, \tag{46a}$$

$$V_{Gp} = V_{DD} - V_{in} - V_{inq}. \tag{46b}$$

where V_{inq} is defined as the quiescent gate voltage for $V_{in} = 0$ such that the output current is zero and hence $I_p = I_n = I_b$ which is given by

$$I_b = I_{D0n} \cdot \mathrm{e}^{\frac{-V_{inq}}{n_n U_T}} = I_{D0p} \cdot \mathrm{e}^{\frac{V_{DD}-V_{inq}}{n_p U_T}}. \tag{47}$$

We can then express I_{D0n} and I_{D0p} as

$$I_{D0n} = I_b \cdot \mathrm{e}^{\frac{V_{inq}}{n_n U_T}}, \tag{48a}$$

$$I_{D0p} = I_b \cdot \mathrm{e}^{\frac{V_{inq}-V_{DD}}{n_p U_T}}. \tag{48b}$$

$$I_n = I_b \cdot \mathrm{e}^{\frac{V_{inq}}{n_n U_T}} \cdot \mathrm{e}^{\frac{V_{in}-V_{inq}}{n_n U_T}} = I_b \cdot \mathrm{e}^{\frac{V_{in}}{n_n U_T}}, \tag{49a}$$

$$I_p = I_b \cdot \mathrm{e}^{\frac{V_{inq}-V_{DD}}{n_p U_T}} \cdot \mathrm{e}^{\frac{V_{DD}-V_{in}-V_{inq}}{n_p U_T}} = I_b \cdot \mathrm{e}^{\frac{-V_{in}}{n_p U_T}}, \tag{49b}$$

The output current can then be written as

$$I_{out} = I_p - I_n = I_b \cdot \left[\mathrm{e}^{\frac{-V_{in}}{n_n U_T}} - \mathrm{e}^{\frac{V_{in}}{n_n U_T}}\right]. \tag{50}$$

Assuming that $n_n = n_p = n$, the normalized output current can be written as

$$i_{out} \triangleq \frac{I_{out}}{I_b} = -\sinh(v_{in}) \tag{51}$$

where $v_{in} \triangleq V_{in}/(nU_T)$. The normalized output current is plotted in Fig. 5 together with the current of the nMOS and pMOS transistors. We see that the current is ideally not limited hence the inverter can operate as a class AB transconductance amplifier. The current will be limited by the supply voltage and the supply series resistances.

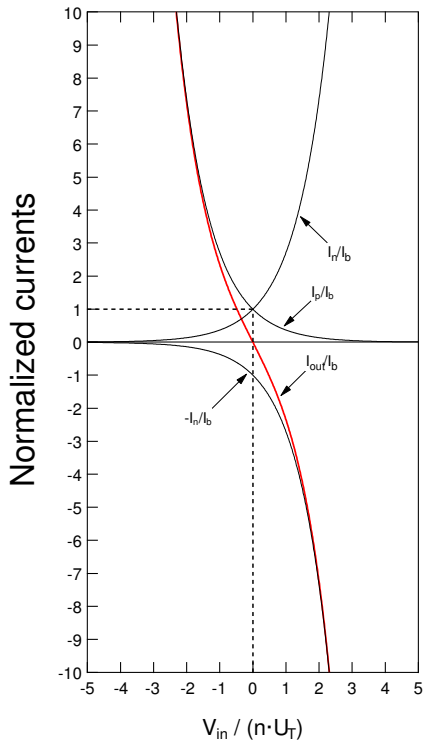

Figure 5: The inverter large signal transfer characteristic in weak inversion.

Problem 3 Effect of velocity saturation on the gate transconductance

3.1 Long-channel case

For the long-channel case the normalized source transconductance only depends on IC and is given by

$$g_{ms} = \frac{\sqrt{4IC+1}-1}{2} = 5. \tag{52}$$

Knowing the bias current $I_b = 1\ \mu A$ and the inversion coefficient we ca deduce the specific current I_{spec} as

$$I_{spec} = \frac{I_b}{IC} = 667\ nA. \tag{53}$$

The gate transconductance is then given by

$$G_m = \frac{I_{spec}}{n \cdot U_T} = 98.6\ \frac{\mu A}{V}. \tag{54}$$

The corresponding bandwidth is then given by

$$BW = \frac{G_m}{2\pi\ C_L} = 3.1\ MHz. \tag{55}$$

3.2 Short-channel case

For the short-channel case, the normalized source transconductance now also depends on the velocity saturation parameter $\lambda_c = 1/3$ according to

$$g_{ms} = \frac{\sqrt{4IC + 1 + (\lambda_c\, IC)^2} - 1}{2 + \lambda_c^2\, IC}. \tag{56}$$

Keeping the same current $I_b = 20\,\mu A$ and inversion coefficient $IC = 30$ with $\lambda_c = 1/3$ results in $g_{ms} = 2.6$, which is 1.92 times smaller than the value obtained for the long-channel case. Assuming the I_{spec} remains the same, we get

$$G_m = \frac{I_{spec}}{n \cdot U_T} = 51.3\,\frac{\mu A}{V}, \tag{57}$$

which is about 1.92 times smaller than what we get for the long-channel case. The corresponding bandwidth is now reduced to

$$BW = \frac{G_m}{2\pi\, C_L} = 1.6\,MHz. \tag{58}$$