Fundamentals of Analog & Mixed Signal VLSI Design
Exercise 10 (27.11.2024)

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Problem 1 Fully Differential Simple OTA

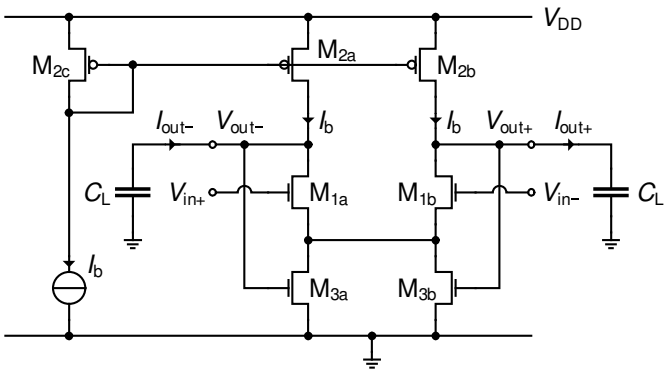

Figure 1: Schematic of the fully differential simple OTA.

In many mixed-signal circuits, the amplifiers are fully differential amplifiers. This means that not only the input is differential but they also have a differential output. There are many advantages of using fully-differential amplifiers, including:

- Reject any common-mode disturbances,
- Provide larger output swing,
- Avoid poles from current mirrors, thus achieving higher closed-loop speed.

However, the DC output common-mode voltage is not defined and needs to be stabilized and set at a common-mode voltage, which requires additional common-mode feedback (CMFB) circuits and hence additional power consumption. Therefore, the extra power consumption needed for the CMFB is an important specifications.

Additionally, the bandwidth of the closed-loop CMFB circuit needs to be sufficiently large to avoid both output to saturate for a long-time making the amplifier out of order for the differential signal. This means that the open-loop gain-bandwidth product of the CMFB circuit GBW_{cm} needs to be at least as high as the gain-bandwidth product in differential mode GBW_{dm}, i.e. $GBW_{dm} \leq GBW_{cm}$. Indeed, if the common-mode gain-bandwidth product GBW_{cm} is much smaller than GBW_{dm}, a fast and large common-mode signal at the amplifier input could saturate the amplifier outputs. Since the CMFB is slow, it takes time to recover, making the amplifier useless during this time. Requiring the GBW_{cm} to be as large as the GBW_{dm} will require a lot of power. Of course it depends on how the CMFB is implemented but usually fully-differential amplifiers consume about the double than their equivalent single-ended amplifiers.

Another limitation of the CMFB is matching. If there is mismatch in the CMFB circuit, the common-mode input signal generates a differential output voltage which translates into distortion. This feature is assessed by the common-mode rejection ratio *CMRR* defined as the ratio of the differential voltage gain to the differential-to-common-mode voltage

gain. Ideally, if there is no mismatch, the differential-to-common-mode voltage gain is zero resulting in an infinite *CMRR*.

Fig. 1 presents the schematic of a fully-differential simple OTA which does not need any additional current for the CMFB. Transistors M_{3a} and M_{3b} are connected to the positive and negative outputs to establish the output common-mode voltage. The output common-mode voltage is extracted from M_{3a} and M_{3b} which operate in the linear region. They change the voltage at the common-source node and therefore also at the output through the action of M_{1a} and M_{1b}.

- What is approximately the level of the common-mode output voltage $V_{oc} \triangleq (V_{out+} + V_{out-})/2$?
- Derive the differential-mode transconductance G_{md} and the differential gain-bandwidth product GBW_{dm} assuming the transistors in the left branch are perfectly matched to those in the right branch.
- Calculate the common-mode transconductance G_{mc} in open-loop. To do this you need to disconnect the gates of M_{3a} and M_{3b} from the outputs. The open-loop common-mode transconductance is then obtained by applying a common-mode voltage at the gates of M_{3a} and M_{3b} and measuring the common-mode output current.
- How do they compare?
- Calculate the small-signal differential DC voltage gain $A_{vd} \triangleq \Delta V_{od}/\Delta V_{id}$ where $V_{id} \triangleq V_{in+} - V_{in-}$ and $V_{od} \triangleq V_{out+} - V_{out-}$ are the input and output differential voltages assuming the transistors in the left branch are perfectly matched to those in the right branch.
- Calculate the small-signal common-mode DC voltage gain $A_{vc} \triangleq \Delta V_{oc}/\Delta V_{ic}$ where $V_{ic} \triangleq (V_{in+} + V_{in-})/2$ and $V_{oc} \triangleq (V_{out+} + V_{out-})/2$ are the input and output common-mode voltages assuming the transistors in the left branch are perfectly matched to those in the right branch.
- Calculate the common-mode to differential-mode voltage gain $A_{cd} \triangleq \Delta V_{od}/\Delta V_{ic}$ assuming there is a G_m-mismatch between M_{1a} and M_{1b}.
- Calculate the corresponding *CMRR*.
- Propose a way to improve the CMFB offering a better control on the output common-mode voltage without increasing the current consumption.

Problem 2 Fully Differential Folded Cascode OTA

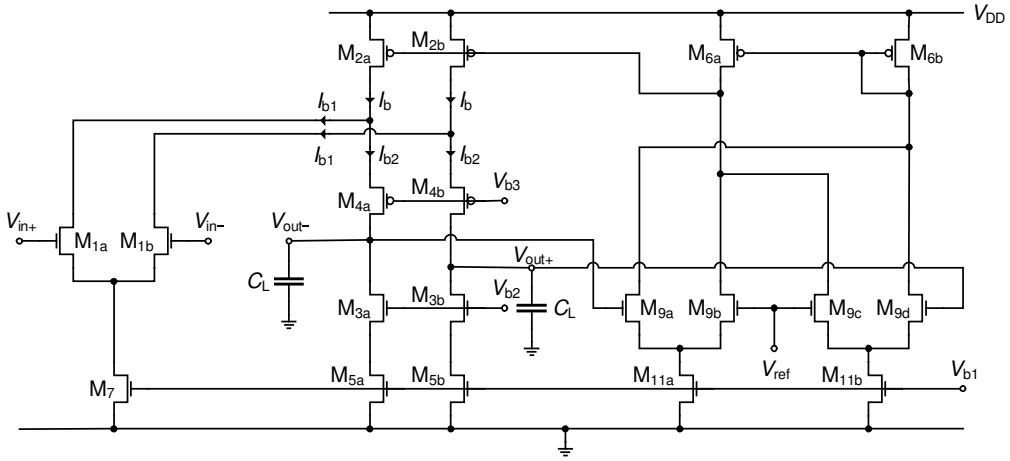

Figure 2: Schematic of the fully differential folded cascode OTA including the CMFB circuit.

Fig. 2 presents a fully differential folded-cascode OTA. The common-mode voltage is extracted by differential pairs M_{9a}-M_{9b} and M_{9c}-M_{9d} and compared to the common-mode reference voltage V_{ref}. If the output common-mode voltage is different from V_{ref}, it is then adjusted by means of the current sources M_{2a}-M_{2b} to bring it back to V_{ref}. To analyze the CMFB, we will derive the open-loop gain (actually transconductance) by opening the loop at the input of the CMFB circuit (i.e. disconnecting the gates of M_{9a} and M_{9d}).

- What is the level of the common-mode output voltage $V_{oc} \triangleq (V_{out+} + V_{out-})/2$?
- Derive the differential-mode transconductance G_{md} and the differential gain-bandwidth product GBW_{dm} assuming the transistors in the left and right branches are perfectly matched.
- Calculate the DC open-loop common-mode transconductance $G_{mc} \triangleq \Delta I_{out}/\Delta V_{in}$ and gain bandwidth product GBW_{cm} assuming again that the transistors in the left and right branches are perfectly matched.
- How do they compare?
- What is the total current consumption for $GBW_{cm} > GBW_{dm}$? How much is the current penalty compared to the single-ended case?

Solutions to Exercise 10 (27.11.2024)

Problem 1 Fully Differential Simple OTA

- What is approximately the level of the common-mode output voltage $V_{oc} \triangleq (V_{out+} + V_{out-})/2$?

Assuming that the transistors of the left and right branches are perfectly matched, then the output common-mode voltage will actually be set by the V_{BG} voltage of M_{2c} which is given by

$$V_{BG2} = V_{T0p} + \sqrt{\frac{2n_2\, I_b}{\beta_2}}. \tag{1}$$

The output common-mode voltage is then approximately given by

$$V_{oc} \cong V_{DD} - V_{BG2} \cong V_{DD} - V_{T0p} - \sqrt{\frac{2n_2\, I_b}{\beta_2}}. \tag{2}$$

We see that the output common-mode voltage is strongly dependent on technology parameters such as V_{T0p} and $\mu\, C_{ox}$. This should be avoided. The next circuit will show an example of how to better control the output common-mode voltage which is independent of the technology parameters and is only limited by matching.

- Derive the differential-mode transconductance G_{md} and the differential gain-bandwidth product GBW_{dm} assuming the transistors in the left branch are perfectly matched to those in the right branch.

In differential mode and assuming that the transistors in the left and right branches are perfectly matched, the common-source node of the differential pair stays constant and can be considered as a small-signal AC ground. The differential-mode transconductance is then simply equal to the transconductance of M_{1a}

$$G_{md} = G_{m1}. \tag{3}$$

The corresponding differential-mode gain-bandwidth product is then simply

$$GBW_{dm} = \frac{G_{m1}}{C_L}. \tag{4}$$

- Calculate the common-mode transconductance G_{mc} in open-loop. To do this you need to disconnect the gates of M_{3a} and M_{3b} from the outputs. The open-loop common-mode transconductance is then obtained by applying a common-mode voltage at the gates of M_{3a} and M_{3b} and measuring the common-mode output current.

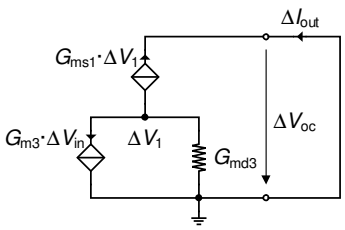

Figure 3: Small-signal schematic for calculating the open-loop common-mode transconductance G_{mc}.

To calculate the open-loop common-mode transconductance G_{mc} we disconnect the gates of M_{3a} and M_{3b} from the outputs and connect them to a input voltage ΔV_{in}. Assuming that the transistors in the left and right branches are

perfectly matched and neglecting the output conductances, we get then equivalent circuit shown in **??**. Analyzing this circuit we obtain the open-loop common-mode transconductance as

$$G_{mc} = \frac{G_{m3}\, G_{ms1}}{G_{md3} + G_{ms1}} = \frac{G_{m3}}{1 + G_{md3}/G_{ms1}}. \tag{5}$$

This seems reasonable since the input voltage ΔV_{in} is first transformed into a current through G_{m3} and then to the voltage ΔV_1 by the load conductance $G_{md3} + G_{ms1}$ and finally to the output current by G_{ms1}. If we assume that M_{3a} and M_{3b} are biased in strong inversion and in the linear region, then

$$G_{m3} = \beta_3 \cdot V_{D3}, \tag{6a}$$
$$G_{md3} = n_3 \cdot \beta_3 \cdot (V_{P3} - V_{D3}) \cong \beta_3 \cdot (V_{G3} - V_{T0n} - n_3 \cdot V_{D3}). \tag{6b}$$

The gate voltage of M_{3a}-M_{3b} is equal to the output common-mode voltage V_{oc}.

If we assume that M_{1a}-M_{1b} are biased in strong inversion then

$$G_{ms1} = n_1 \cdot \beta_1 \cdot (V_{P1} - V_{S1}) = n_1 \cdot \beta_1 \cdot (V_{P1} - V_{D3}) = \beta_1 \cdot (V_{ic} - V_{T0n} - n_1 \cdot V_{D3}) \tag{7}$$

Assuming that $n_1 = n_3$, we get

$$\frac{G_{md3}}{G_{ms1}} = \frac{\beta_3 \cdot (V_{oc} - V_{T0n} - n \cdot V_{D3})}{\beta_1 \cdot (V_{ic} - V_{T0n} - n \cdot V_{D3})}. \tag{8}$$

Assuming that the output common-mode voltage is set to the input common-mode voltage $V_{oc} = V_{ic}$

$$\frac{G_{md3}}{G_{ms1}} \cong \frac{\beta_3}{\beta_1}. \tag{9}$$

If $\beta_1 \gg \beta_3$, then $G_{md3}/G_{ms1} \ll 1$ and

$$G_{mc} \cong G_{m3}. \tag{10}$$

The corresponding common-mode gain-bandwidth product is then given by

$$GBW_{cm} = \frac{G_{mc}}{C_L} = \frac{G_{m3}\, G_{ms1}}{C_L\,(G_{md3} + G_{ms1})}. \tag{11}$$

In the case $G_{md3} \ll G_{ms1}$, then

$$GBW_{cm} \cong \frac{G_{m3}}{C_L}. \tag{12}$$

- How do they compare?

The ratio G_{md}/G_{mc} is given by

$$\frac{G_{md}}{G_{mc}} = \frac{G_{md3} + G_{ms1}}{n_1\, G_{m3}}. \tag{13}$$

Assuming again that $G_{md3} \ll G_{ms1}$, we have

$$\frac{G_{md}}{G_{mc}} \cong \frac{G_{m1}}{G_{m3}}. \tag{14}$$

where we have used $G_{ms1} = n_1 \cdot G_{m1}$. Assuming again that M_{1a}-M_{1b} are biased in strong inversion then

$$G_{m1} = \beta_1 \cdot (V_{P1} - V_{S1}) = \beta_1 \cdot (V_{P1} - V_{D3}) = \frac{\beta_1}{n_1} \cdot (V_{ic} - V_{T0n} - n_1 \cdot V_{D3}) \tag{15}$$

and

$$\frac{G_{md}}{G_{mc}} \cong \frac{\beta_1}{\beta_3} \cdot \left(\frac{V_{P3}}{V_{D3}} - 1\right) = \frac{\beta_1}{\beta_3} \cdot \left(\frac{V_{ic} - V_{T0n}}{n_1 \cdot V_{D3}} - 1\right), \tag{16}$$

which is usually larger than 1. This means that the common-mode gain-bandwidth GBW_{cm} is unavoidably smaller than the differential-mode gain-bandwidth product GBW_{dm} which is not desired.

- Calculate the small-signal differential DC voltage gain $A_{vd} \triangleq \Delta V_{od}/\Delta V_{id}$ where $V_{id} \triangleq V_{in+} - V_{in-}$ and $V_{od} \triangleq V_{out+} - V_{out-}$ are the input and output differential voltages assuming the transistors in the left branch are perfectly matched to those in the right branch.

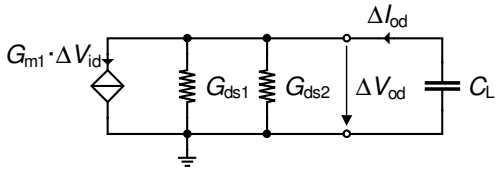

Figure 4: Small-signal schematic for calculating the differential voltage gain.

The small-signal circuit in differential mode assuming that the left and right branches are perfectly matched is shown in **??**. The small-signal differential voltage gain is then given by

$$A_{vd} \triangleq \frac{\Delta V_{od}}{\Delta V_{id}} = \frac{A_{vd0}}{1 + s/\omega_{c,dm}} \tag{17}$$

where

$$A_{vd0} \cong -\frac{G_{m1}}{G_{ds1} + G_{ds2}}, \tag{18a}$$

$$\omega_{c,dm} \cong \frac{G_{ds1} + G_{ds2}}{C_L}. \tag{18b}$$

are the differential-mode DC gain and bandwidth, respectively. The gain-bandwith product is equal to

$$GBW_{dm} = |A_{vd0}| \cdot \omega_{c,dm} = \frac{G_{m1}}{C_L}, \tag{19}$$

which is consistent with the result found above.

- Calculate the small-signal common-mode DC voltage gain $A_{vc} \triangleq \Delta V_{oc}/\Delta V_{ic}$ where $V_{ic} \triangleq (V_{in+} + V_{in-})/2$ and $V_{oc} \triangleq (V_{out+} + V_{out-})/2$ are the input and output common-mode voltages assuming the transistors in the left branch are perfectly matched to those in the right branch.

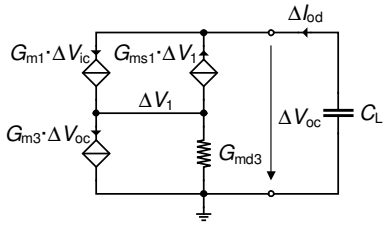

Figure 5: Small-signal schematic of the fully differential simple OTA in common-mode operation (closed-loop).

Assuming again that the transistors in the left and right branches are perfectly matched and neglecting the output conductances, the small-signal circuit in common-mode operation simplifies to **??**. The common-mode voltage gain is then given by

$$A_{vc} \triangleq \frac{\Delta V_{oc}}{\Delta V_{ic}} = \frac{A_{vc0}}{1 + s/\omega_{c,cm}}. \tag{20}$$

where

$$A_{vc0} \cong -\frac{G_{md3}}{n_1\, G_{m3}}, \tag{21a}$$

$$\omega_{c,cm} \cong \frac{G_{m3}\, G_{ms1}}{(G_{md3} + G_{ms1})\, C_L}. \tag{21b}$$

are the common-mode DC gain and bandwidth, respectively. Note that, since the feedback gain is unity, the bandwidth $\omega_{c,cm}$ actually corresponds to the open-loop common-mode gain-bandwidth product GBW_{cm} calculated above.

Reusing **??** and assuming $n_3 \cong n_1$, the DC common-mode voltage gain is given by

$$A_{vc0} \cong 1 - \frac{V_{P3}}{V_{D3}}. \tag{22}$$

Usually, V_{P3} cannot be made much larger than V_{D3} and therefore the common-mode DC gain remains small, which is not really a problem. It is actually even better because if the coomon-mode gain is small, any common-mode error at the input does not propagate to the output.

- Calculate the common-mode to differential-mode voltage gain $A_{cd} \triangleq \Delta V_{od}/\Delta V_{ic}$ assuming there is a G_m-mismatch between M_{1a} and M_{1b}.

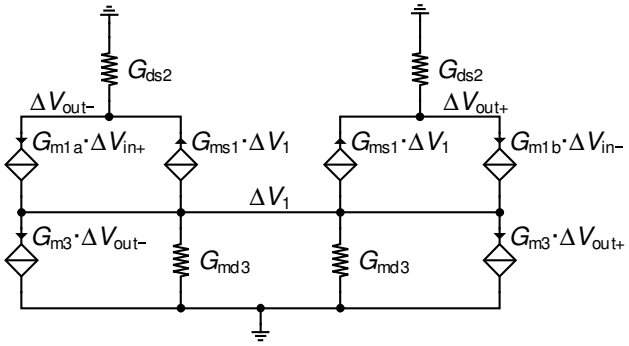

Figure 6: Small-signal schematic of the fully differential simple OTA to calculate the common-mode to differential-mode voltage gain due to a G_{m1} mismatch.

To calculate the effect of the G_m mismatch in the differential pair, we use the small-signal schematic shown in **??**. Assuming that all the components are symmetrical except for G_{m1a} and G_{m1b}, the common-mode to differential-mode voltage gain is given by

$$A_{vcd} \triangleq \frac{V_{od}}{V_{ic}} = \frac{\Delta G_{m1}}{G_{ds1} + G_{ds2}}, \tag{23}$$

where $\Delta G_{m1} = G_{m1a} - G_{m1b}$.

- Calculate the corresponding *CMRR*.

The *CMRR* is then simply given by

$$CMRR = \left(\frac{\Delta G_{m1}}{G_{m1}}\right)^{-1}. \tag{24}$$

The CMRR is therefore equal to the inverse of the relative G_m-mismatch.

- Propose a way to improve the CMFB offering a better control on the output common-mode voltage without increasing the current consumption.

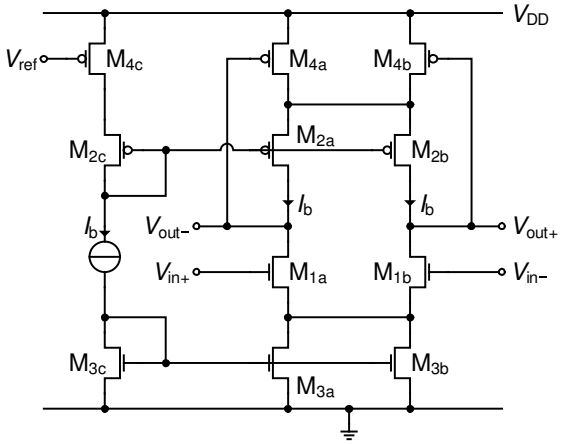

Figure 7: Fully differential simple OTA with a CMFB controlling the output common-mode from the top current sources.

The CMFB can be improved by adjusting the common-mode current from the top instead of from the bottom as shown in **??**. With this CMFB circuit, the output common-mode voltage is set to the reference voltage V_{ref} by matching of the gate voltages of M_{4a}, M_{4b} and M_{4c}. It therefore does not depend on the process parameters as in the circuit of Fig. 1 but is limited by transistor matching. However, the common-mode transconductance and gain-bandwidth product is identical to those obtained for the circuit of Fig. 1. Another CMFB circuit allowing to set the common-mode transconductance and gain-bandwidth product independently of that of the differential mode is discussed below.

Problem 2 Fully Differential Folded Cascode OTA

- What is the level of the common-mode output voltage $V_{oc} \triangleq (V_{out+} + V_{out-})/2$?

Contrary to the CMFB of Fig. 1, the output common-mode voltage is set to V_{ref} by the CMFB and does not depend on the process parameters. The control of the output common-mode voltage is limited by transistor matching.

- Derive the differential-mode transconductance G_{md} and the differential gain-bandwidth product GBW_{dm} assuming the transistors in the left and right branches are perfectly matched.

The differential transconductance G_{md} is simply equal to G_{m1}. The differential gain-bandwidth product is therefore equal to

$$GBW_{dm} = \frac{G_{m1}}{C_L}. \tag{25}$$

- Calculate the DC open-loop common-mode transconductance $G_{mc} \triangleq \Delta I_{out}/\Delta V_{in}$ and gain bandwidth product GBW_{cm} assuming again that the transistors in the left and right branches are perfectly matched.

The DC common-mode transconductance is calculated by opening the loop at the gates of M_{9a} and M_{9d} connecting them together and applying an input voltage ΔV_{in}. It is given by

$$G_{mc} = \frac{\Delta I_{D2}}{\Delta V_{in}} = G_{m2} \cdot A_{cm} \tag{26}$$

where A_{cm} is the voltage gain of the differential difference amplifier

$$A_{cm} = \frac{G_{m9}}{G_o} \tag{27}$$

where G_o is the total conductance at the drains of M_{9b} and M_{9c}. Finally, the common-mode gain-bandwidth product is simply given by

$$GBW_{cm} = \frac{G_{mc}}{C_L}. \tag{28}$$

- How do they compare?

In this case, the common-mode gain-bandwidth product can be made larger than the differential-mode gain-bandwidth product by choosing

$$G_{m1} \leq G_{m2} \cdot \frac{G_{m9}}{G_o}. \tag{29}$$

G_{mc} and GBW_{cm} can be made much larger than G_{md} and GBW_{dm} by choosing $G_{m9} = G_{m1}$.

- What is the total current consumption for $GBW_{cm} = GBW_{dm}$? How much is the current penalty compared to the single-ended case?

If we choose $G_{m9} = G_{m1}$, then the bias current of M_{9a}-M_{9b} and M_{9c}-M_{9d} are equal to that of M_{1a}-M_{1b}. This adds 4 I_{b1} to the current consumption. If $I_{b2} = 1.2\ I_{b1}$ then the total current consumption is $I_{tot} = 8.4\ I_{b1}$ compared to 4.4 I_{b1}. The total current is therefore almost doubled.