Fundamentals of Analog & Mixed Signal VLSI Design

Single-ended Differential Amplifier
Part 3

Christian Enz

Integrated Circuits Lab (ICLAB), Institute of Electrical and Micro-Engineering (IEM), School of Engineering (STI)

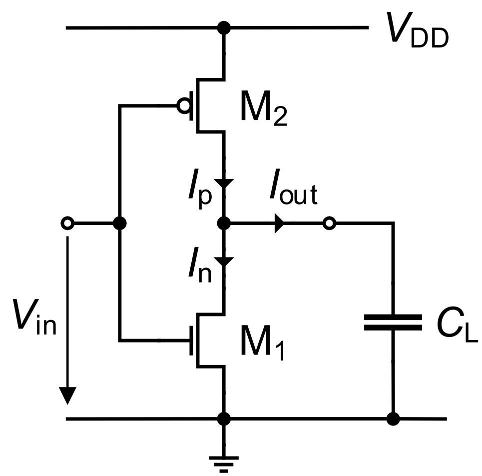
Swiss Federal Institute of Technology, Lausanne (EPFL), Switzerland

EPFL

Outline

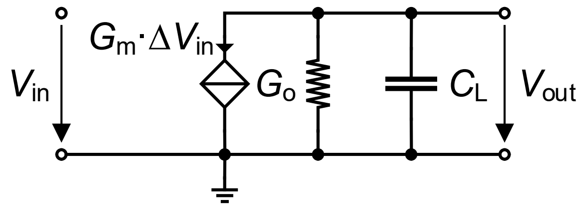
- **The CMOS inverter OTA**
- Improved slew-rate OTAs
- Appendices

The CMOS Inverter as an Amplifier



- The CMOS inverter can be used as a very efficient amplifier thanks to the current sharing between the nMOS and pMOS transistors
- The overall transconductance is the sum of the nMOS and pMOS transconductances
- In WI, the CMOS inverter can operate at very low-voltage thanks to the minimum saturation voltage achieved in WI

The CMOS Inverter – Small-signal and Noise Analysis



- The overall OTA G_m is the sum of the nMOS and pMOS G_m

$$G_m = G_{m1} + G_{m2} \cong 2G_{m1} = 2\,\frac{I_b}{nU_T}$$

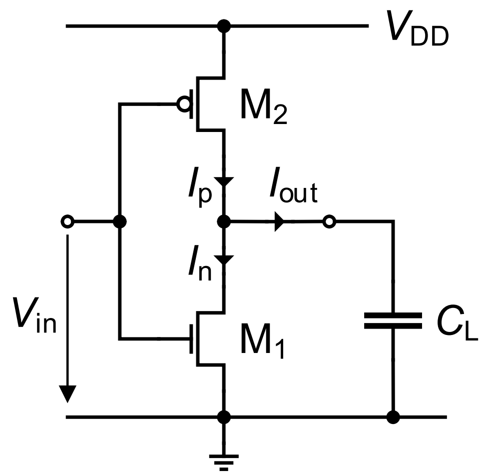
- which in WI is twice that of a single transistor since both transistors share the same bias current
- The DC gain is given by

$$A_{dc} = -\frac{G_m}{G_o} = -\frac{G_{m1} + G_{m2}}{G_{ds1} + G_{ds2}}$$

- and the noise is half that of a single transistor for the same bias current

$$R_n = \frac{G_{n1} + G_{n2}}{(G_{m1} + G_{m2})^2} = \frac{2\,\gamma_{n1} \cdot G_{m1}}{4\,G_{m1}^2} = \frac{\gamma_{n1}}{2G_{m1}} = \frac{R_{n1}}{2}$$

Large-signal Transfer Characteristic in WI



- Assuming that $n_1 = n_2 = n$ the output current $I_{out} = I_p - I_n$ is given by

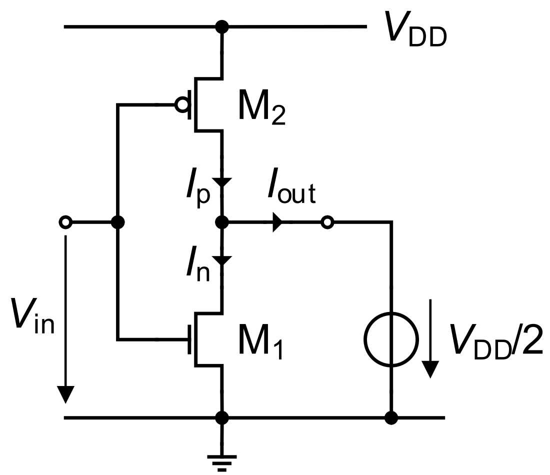
$$i_{out} \triangleq \frac{I_{out}}{I_b} = -2\sinh\left(\frac{V_{in} - V_b}{nU_T}\right)$$

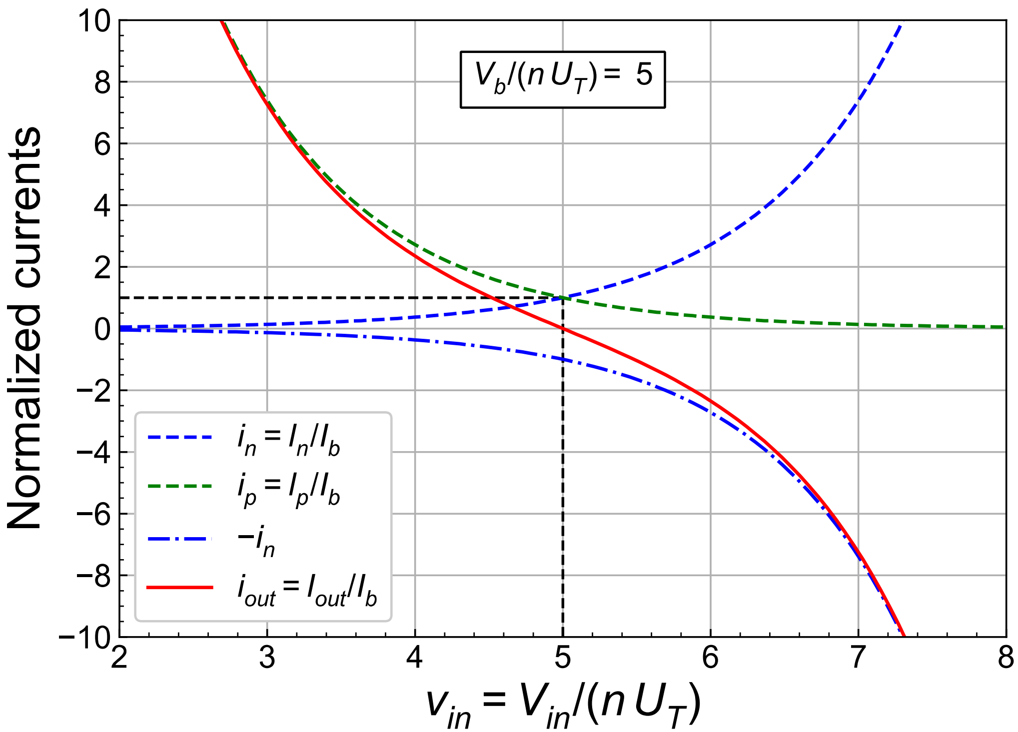
- V_b and I_b correspond to the quiescent gate and bias current for $I_{out} = 0$

$$I_b = I_{D01} \cdot e^{\frac{V_b}{nU_T}} = I_{D02} \cdot e^{\frac{V_{DD}-V_b}{nU_T}}$$

- where $I_{D01} = I_{spec1} \cdot e^{\frac{-V_{T0n}}{nU_T}}$ and $I_{D02} = I_{spec2} \cdot e^{\frac{-V_{T0p}}{nU_T}}$
- with $I_{spec1} = I_{specn\square} \cdot \frac{W_1}{L_1}$ and $I_{spec2} = I_{specp\square} \cdot \frac{W_2}{L_2}$

Class AB Transfer Characteristic

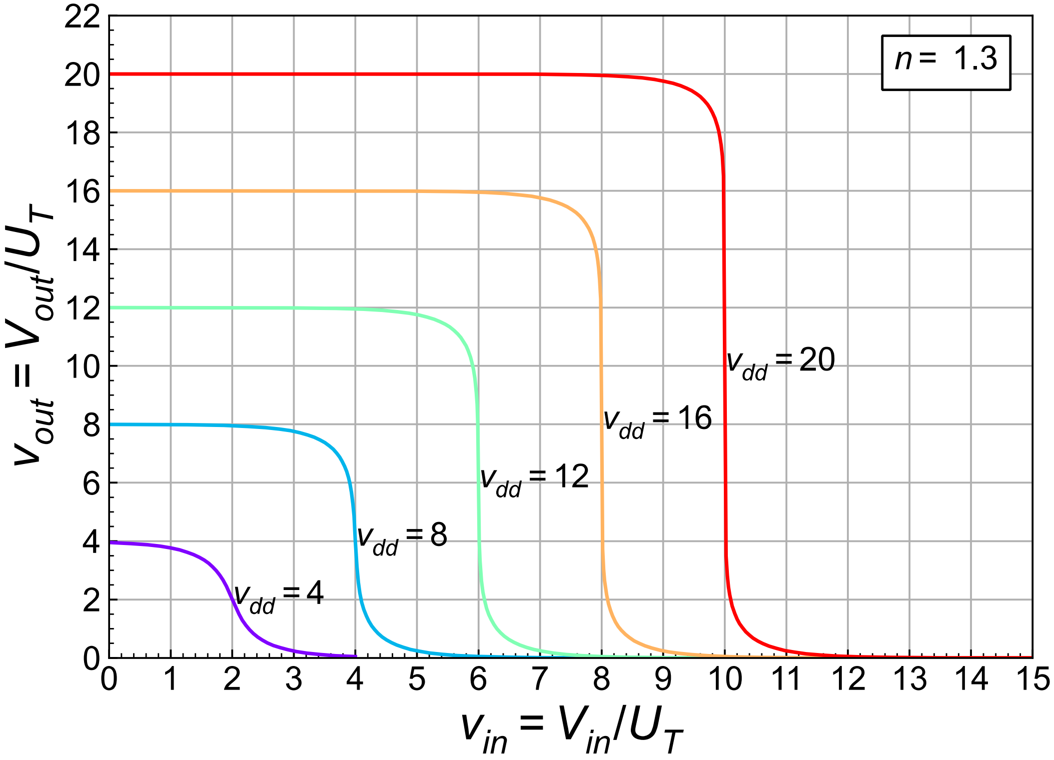




- The current is not limited by a bias current but by the supply voltage
- The class AB transfer characteristic is shown above for the case $V_b = V_{DD}/2$
- The use of inverters was proposed by Krummenacher already in 1981 for designing micropower SC filters

F. Krummenacher, E. Vittoz, and M. Degrauwe, Electronics Letters, 1981.

Large-signal Transfer Characteristic in WI

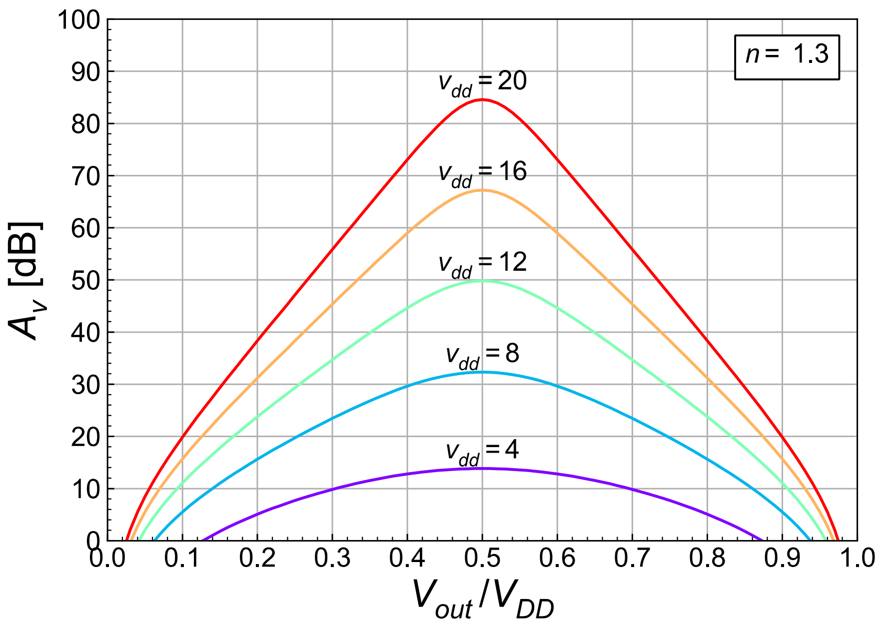


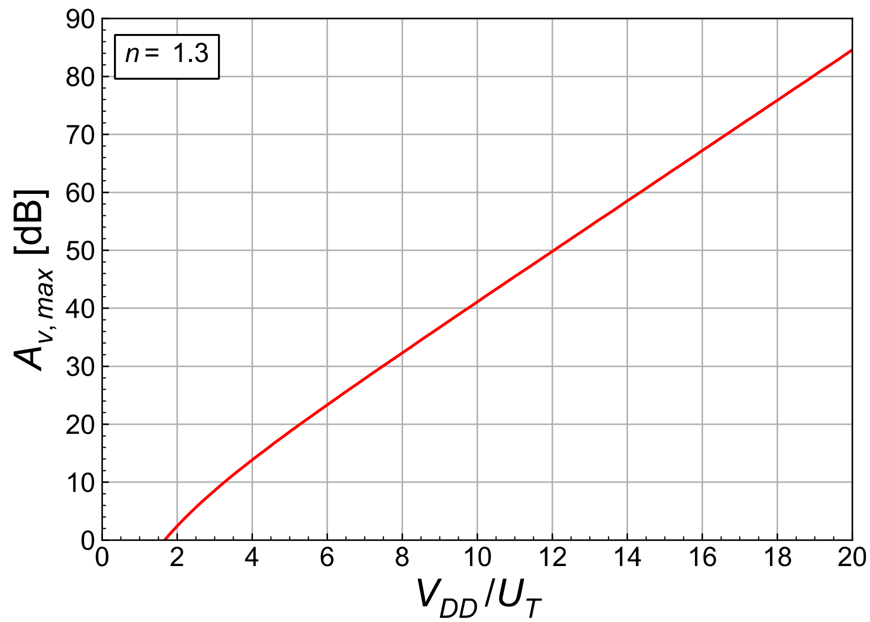
- Assuming $n_1 = n_2 = n$, $I_{D01} = I_{D02}$ and neglecting SCE (DIBL and CLM)
- Can operate at very low supply voltage still providing some voltage gain

E. Vittoz, "Analog Circuits in Weak Inversion" in *Sub-threshold Design for Ultra Low-Power Systems*, Springer 2006.

E. Vittoz, "Weak Inversion for Ultimate Low-Power Logic" in *Low-Power Electronics Design*, Ed. C. Piguet, CRC Press 2005.

Voltage Gain





- Large DC gain can be obtained at very low-voltage, provided
  - low, controlled threshold voltages are available
  - adequate bias scheme is implemented
- Of course the large voltage gain shown above can be significantly lower because of SCE such as DIBL

E. Vittoz, "Analog Circuits in Weak Inversion" in *Sub-threshold Design for Ultra Low-Power Systems*, Springer 2006.
E. Vittoz, "Weak Inversion for Ultimate Low-Power Logic" in *Low-Power Electronics Design*, Ed. C. Piguet, CRC Press 2005.

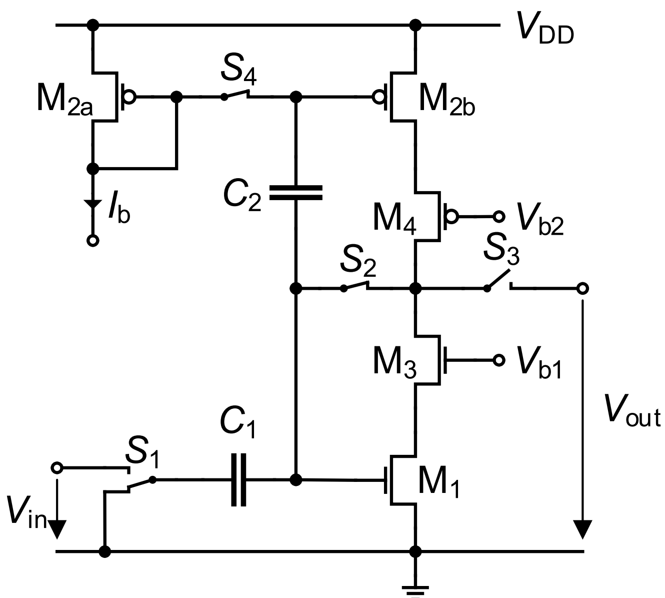
The CMOS Inverter in Weak Inversion

- The CMOS inverter has many great features particularly when it is biased in WI, including:
  - Maximum transconductance at given current I_b
    (global G_m is doubled for the same bias current since in WI $G_m \propto I_b$)
  - Maximum DC gain
  - Minimum input-referred white noise at given current I_b
  - Intrinsically class AB
  - Very low-voltage operation
- However it suffers from a major drawback, namely
  - Poor intrinsic PSRR (6 dB)!
- The later can be circumvented by adding a voltage regulator
- In SI and saturation, for long-channel transistors with for $\beta_1/n_1 = \beta_2/n_2$, the OTA operates as a linear transconductor

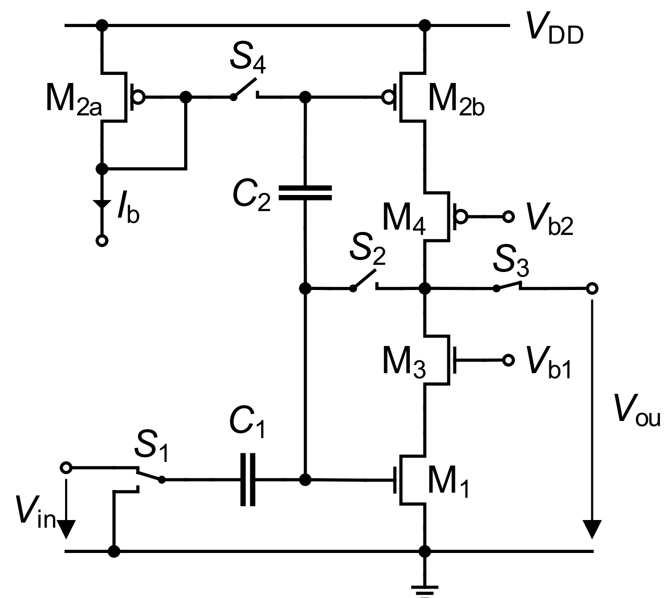
F. Krummenacher, E. Vittoz, and M. Degrauwe, Electronics Letters, 1981.
E. Vittoz, "Analog Circuits in Weak Inversion" in *Sub-threshold Design for Ultra Low-Power Systems*, Springer 2006.

Dynamically Biased Inverter Amplifier (1/2)

Phase Φ_1 (Autozero)



Phase Φ_2 (Amplification)

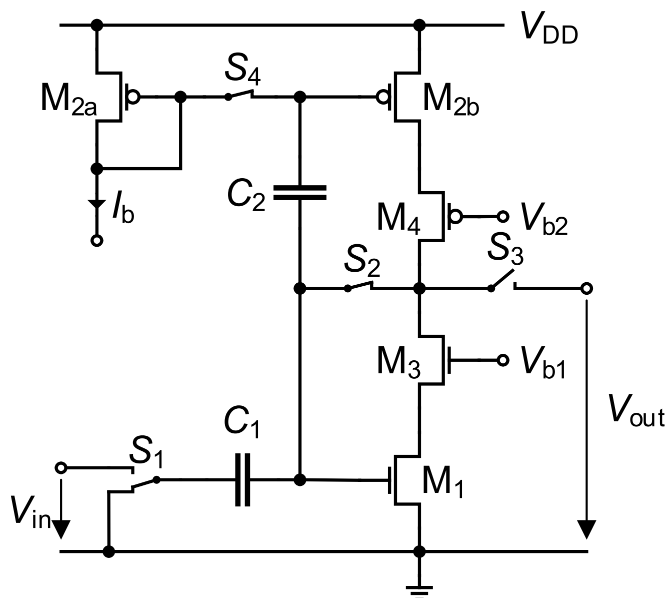


- Two non-overlapping phases operation
- During phase Φ_1, the amplifier is disconnected from the input and the bias current is imposed in the inverter
- At the end of phase Φ_1, the bias voltages are sampled on C_1 and C_2 ideally maintaining the bias current I_b in the inverter during the amplification phase Φ_2

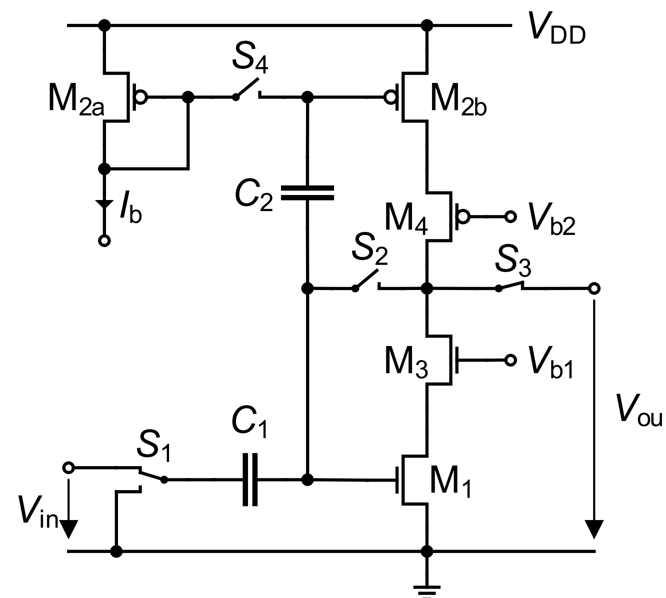
F. Krummenacher, E. Vittoz, and M. Degrauwe, Electronics Letters, 1981.

Dynamically Biased Inverter Amplifier (2/2)

Phase Φ_1 (Autozero)



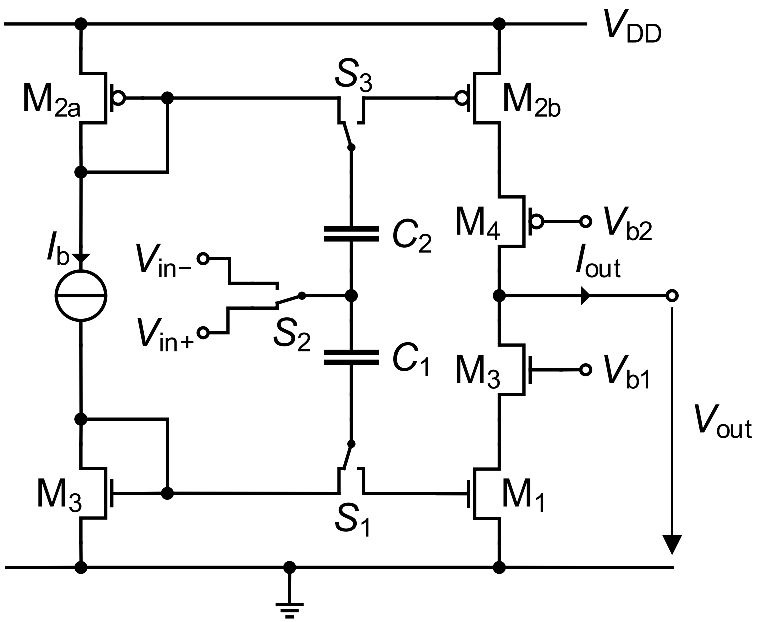
Phase Φ_2 (Amplification)



- Pros:
  - Good low-frequency PSRR
  - No offset
  - Reduction of 1/f noise by autozero
  - Flexible input common-mode
- Cons:
  - Two non-overlapping phases
  - Discontinuous operation
  - Systematic step at output
  - Charge injection

F. Krummenacher, E. Vittoz, and M. Degrauwe, Electronics Letters, 1981.

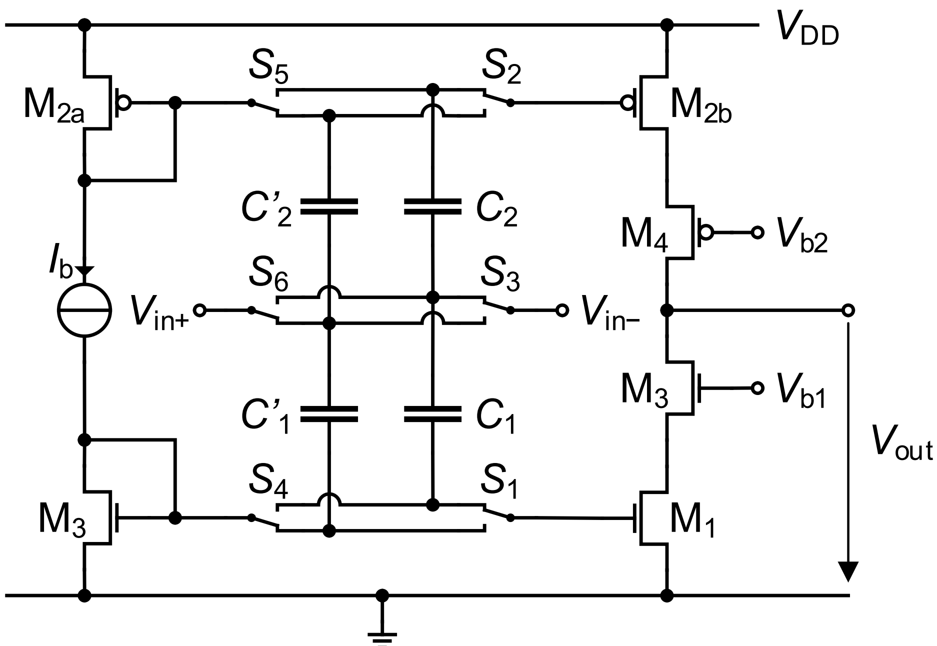
Differential Dynamically Biased Inverter Amplifier



- The above circuit provides a differential input
- In most SC circuits, the positive input is set to a certain commode-mode voltage
- The above circuit samples the bias voltage during phase Φ_1 referenced to the common-mode voltage imposed on the positive input
- The bias voltage sampled on C_1 and C_2 are then applied to M_1 and M_{2b} during the amplification phase Φ_2

S. Masuda, Y. Kitamura, S. Ohya, and M. Kikuchi, “CMOS Sampled Differential, Push Pull Cascode Operational Amplifier,” ISCAS 1984.

Differential Dynamically Biased Inverter Amplifier



- The above circuit can operate during both phases Φ_1 and Φ_2
- Indeed, the amplifier inputs (gates of M_1 and M_{2b}) are always connected to the negative input, while the gates of M_{2a} and M_3 are always connected to the positive input
- This OTA can therefore directly replace the OTAs in SC filters

S. Masuda, Y. Kitamura, S. Ohya, and M. Kikuchi, "CMOS Sampled Differential, Push Pull Cascode Operational Amplifier," ISCAS 1984.

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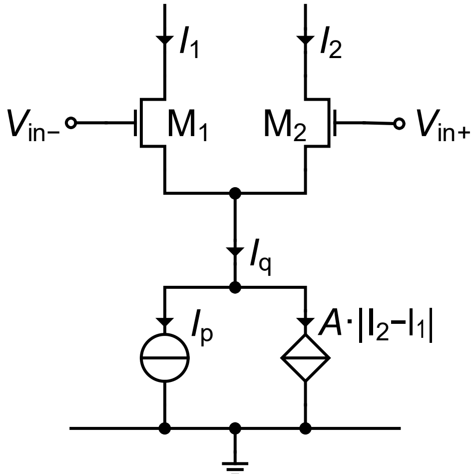
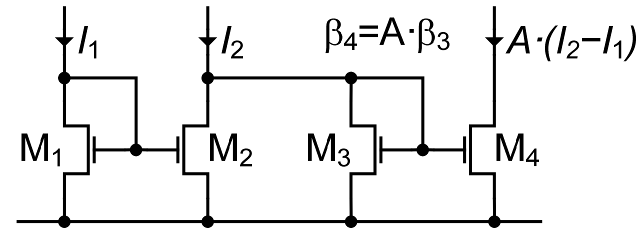
- **Improved slew-rate OTAs**
- Appendices

Differential Feedback Amplifier – Principle





- **Settling time** of simple OTAs having their input differential pair biased in WI is set by the **slew-rate**
- Limited slew rate due to small currents can be circumvented by using **adaptive biasing**
- Principle: increase the differential pair bias current for large differential input signals

$$I_q = I_p + A \cdot |I_2 - I_1| \text{ with } I_q = I_1 + I_2$$

M. Degrauwe, *et al.*, JSSC, 1985

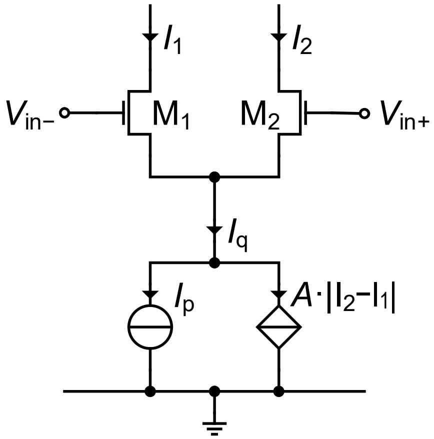
Differential Feedback Amplifier – Output Current

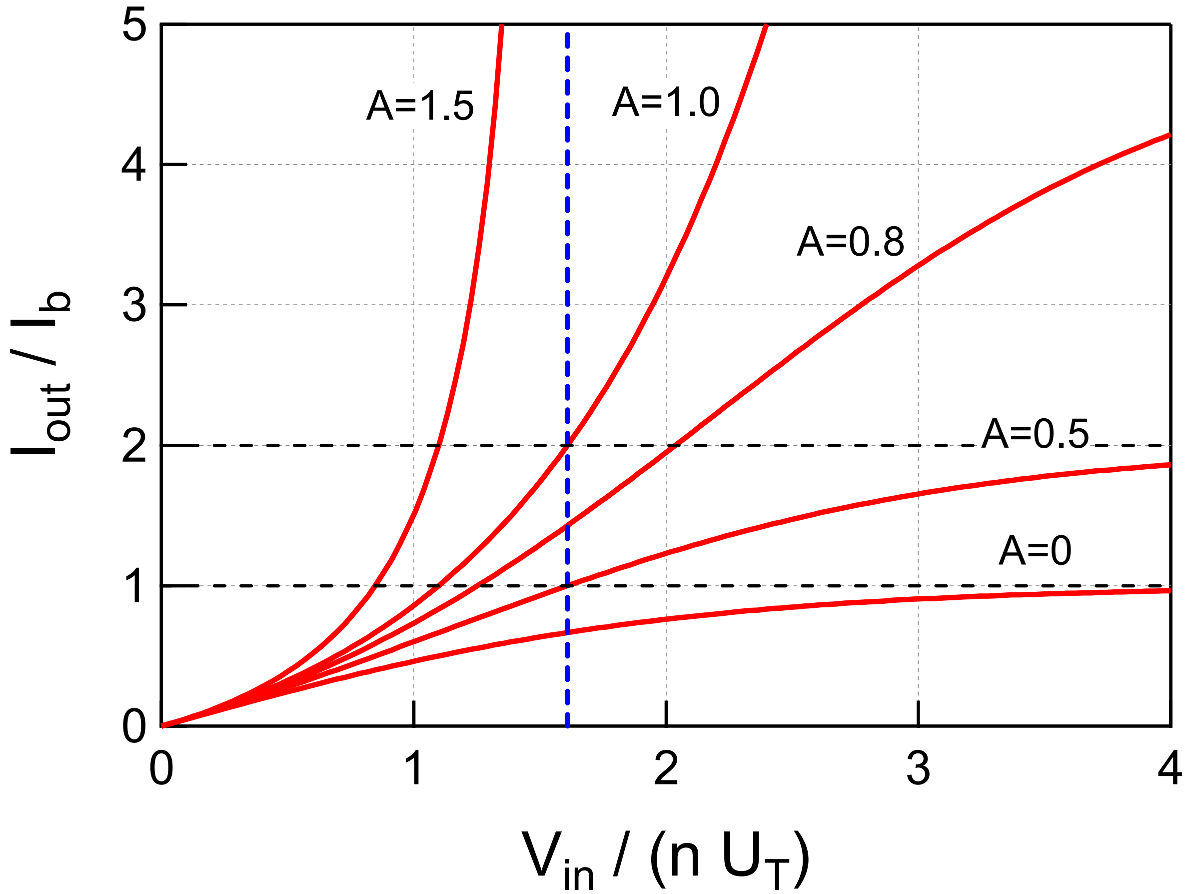
- It can be shown that currents I_1 and I_2 depend on $V_{in} \triangleq V_{in+} - V_{in-}$ according to
$$i_1 \triangleq \frac{I_1}{I_p} = \frac{1}{1+A+(1-A)e^{v_{in}}} \text{ and } i_2 \triangleq \frac{I_2}{I_p} = \frac{e^{v_{in}}}{1+A+(1-A)e^{v_{in}}} \text{ with } v_{in} \triangleq \frac{V_{in}}{nU_T}$$
- Resulting in the output current $I_{out} = I_2 - I_1$ given by
$$i_{out} \triangleq \frac{I_{out}}{I_p} = i_2 - i_1 = \frac{\tanh\left(\frac{v_{in}}{2}\right)}{1 - A\tanh\left(\frac{v_{in}}{2}\right)}$$
- In the particular case where there is no feedback ($A = 0$) we recover the differential pair transfer characteristic
$$i_{out} = \tanh\left(\frac{v_{in}}{2}\right)$$
- For $0 < A < 1$, the output current is limited to $I_p/(1 - A)$
- For $A \geq 1$, the output current is no longer limited to the bias current I_p
- The output current tends to infinity for a critical value of the input voltage given by
$$V_{in,crit} = nU_T \cdot \ln\left(\frac{A+1}{A-1}\right)$$
- For $A = 1$, one of the two branches remains at $I_p/2$ i.e. $min(I_1, I_2) = \frac{I_p}{2}$ and the output current becomes
$$i_{out} = \frac{1}{2}(e^{v_{in}} - 1)$$

M. Degrauwe, *et al.*, JSSC, 1985

Differential Feedback Amplifier – Output Current

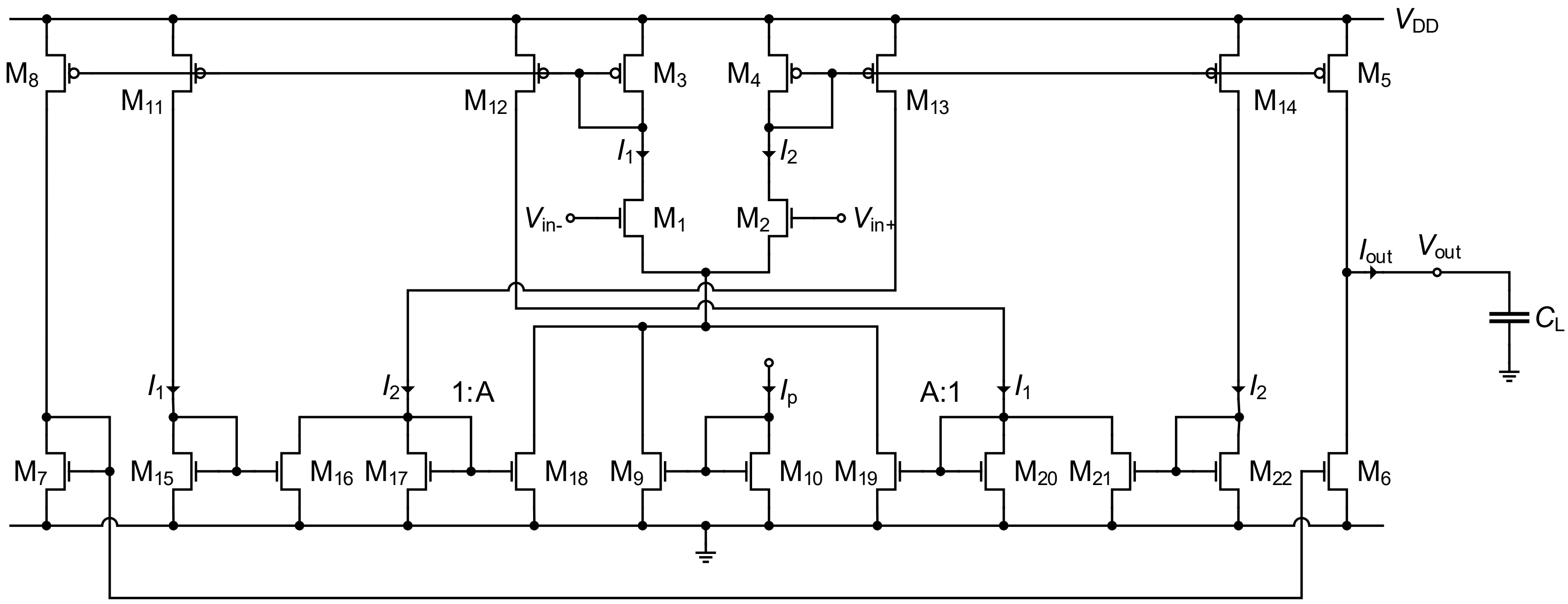
$$I_{out} = I_2 - I_1$$
$$V_{in} = V_{in+} - V_{in-}$$





M. Degrauwe, *et al.*, JSSC, 1985

Differential Feedback Amplifier – Differential OTA



- Transistors M_1 to M_{10} implement the symmetrical OTA, whereas transistors M_{11} to M_{22} implement the two feedback networks

M. Degrauwe, *et al.*, JSSC, 1985

Differential Feedback Amplifier – Experimental Validation

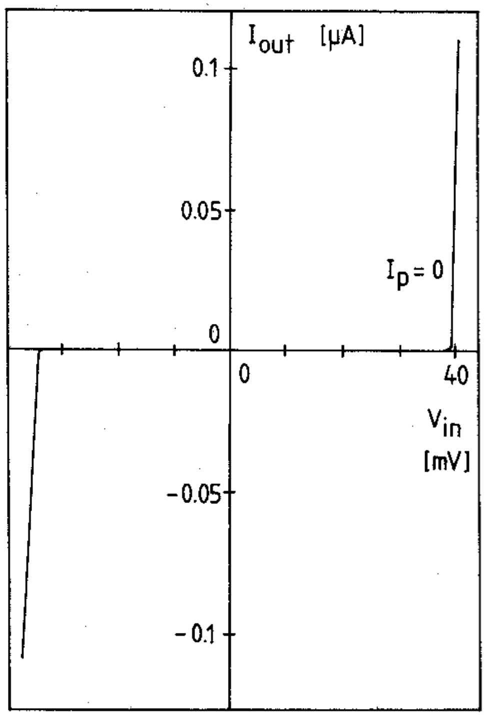


Fig. 8. Measured output current for $I_p = 0$.

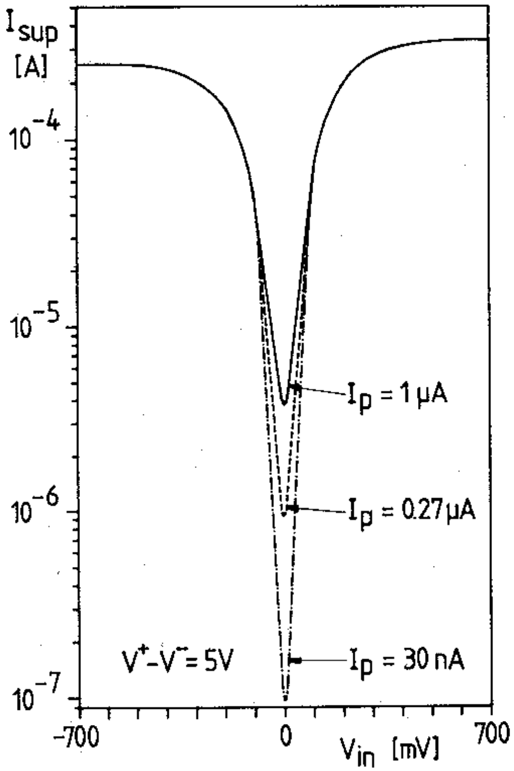
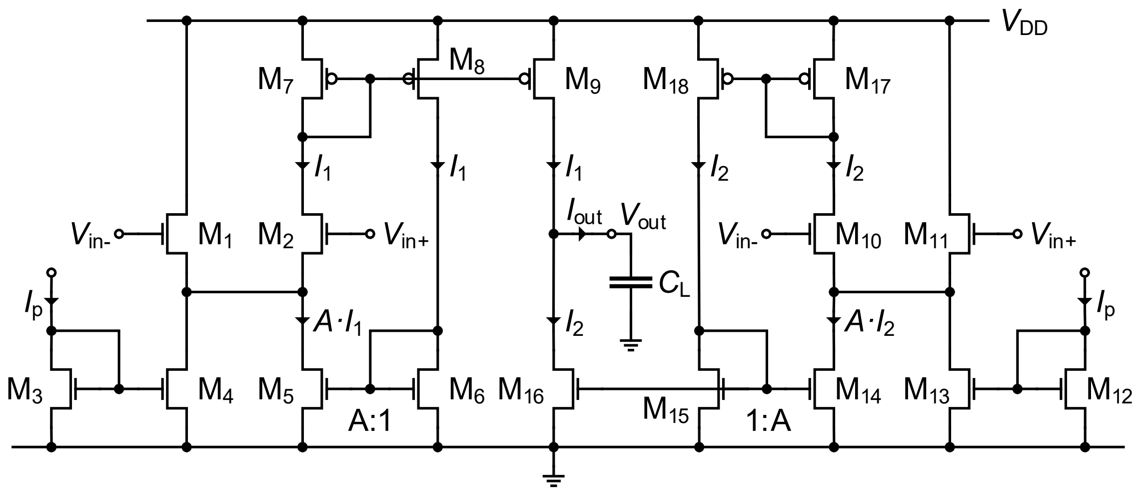


Fig. 9. Supply current as a function of the input signal.

M. Degrauwe, *et al.*, JSSC, 1985

Direct Feedback Amplifier – Principle



- When the differential input voltage $V_{in} = V_{in+} - V_{in-}$ equals zero, the quiescent currents I_1 and I_2 are equal and given by

$$I_{1(2)} = \frac{1}{2} \cdot \left(I_p + A \cdot I_{1(2)}\right)$$

- Which can be solved for I_1 and I_2 resulting in

$$I_1 = I_2 = I_0 = \frac{I_p}{2 - A}$$

- Stability is then insured for a current gain $A < 2$

M. Degrauwe, *et al.*, JSSC, 1985

Direct Feedback Amplifier – Output Current

- It can be shown that currents I_1 and I_2 depend on V_{in} according to

$$i_1 \triangleq \frac{I_1}{I_p} = \frac{1}{1-A+e^{-v_{in}}} \text{ and } i_2 \triangleq \frac{I_2}{I_p} = \frac{1}{1-A+e^{+v_{in}}} \text{ with } v_{in} \triangleq \frac{V_{in}}{nU_T}$$

- Resulting in the output current $I_{out} = I_1 - I_2$ is given by

$$i_{out} \triangleq \frac{I_{out}}{I_p} = i_1 - i_2 = \frac{2\sinh(v_{in})}{1 + (1-A)^2 + 2(1-A)\cosh(v_{in})}$$

- In the particular case where there is no feedback ($A = 0$) we recover the differential pair transfer characteristic

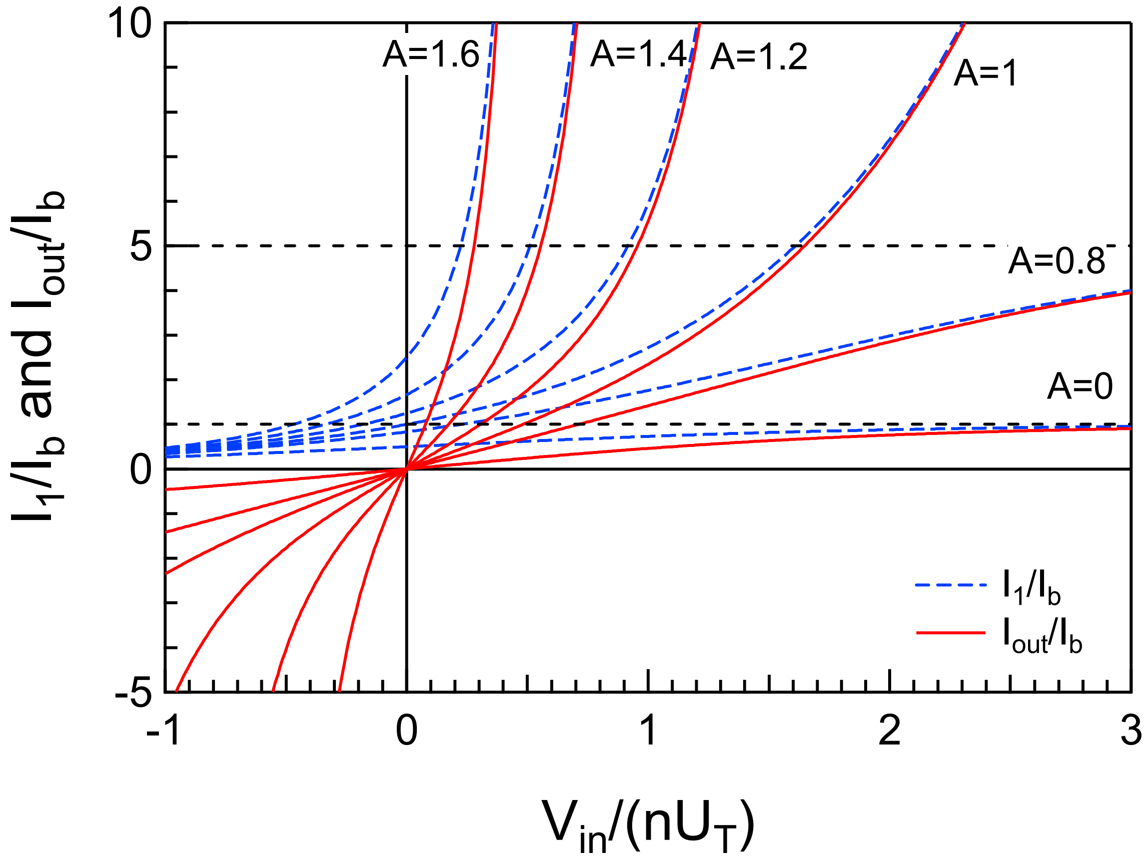
$$i_{out} = \tanh\left(\frac{v_{in}}{2}\right)$$

- For $A < 1$, the output current is limited to $I_p/(1-A)$
- For $A = 1$, the currents become exponential and the output current is no more limited and becomes

$$i_{out} = 2\sinh(v_{in})$$

- For $A > 1$, the current tends to infinity for $v_{in} = \cosh^{-1}\left(\frac{A^2-2A+2}{2(A-1)}\right)$

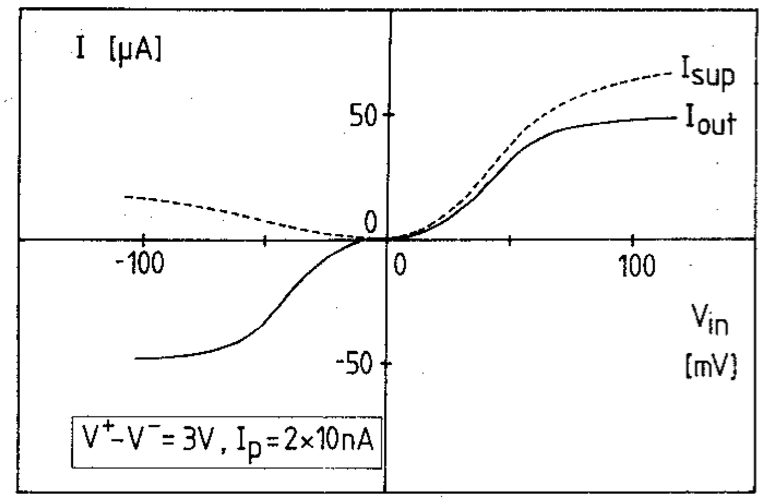
Direct Feedback Amplifier – Output Current

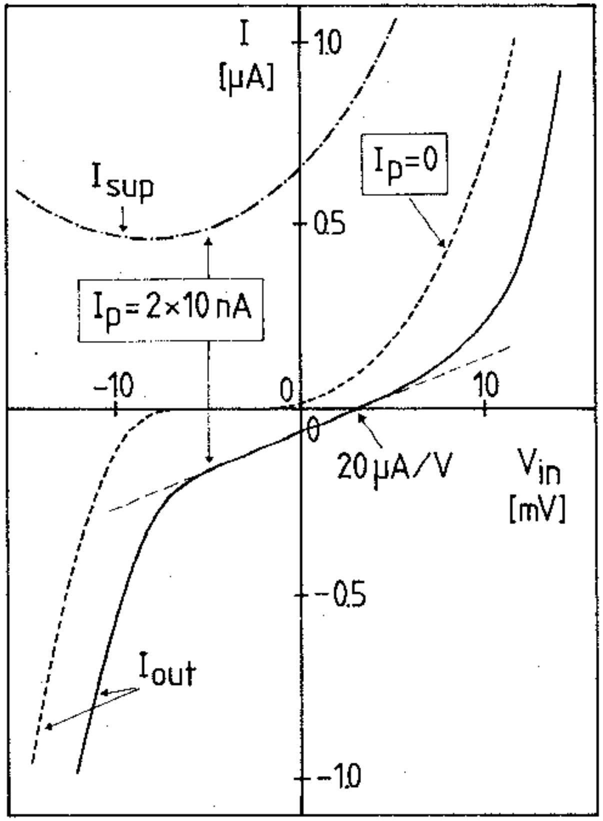


- As shown in the next slide, the output current will be limited by the maximum current that can be provided by the supply

Direct Feedback Amplifier – Experimental Validation

$$A = 1.4$$





M. Degrauwe, *et al.*, JSSC, 1985

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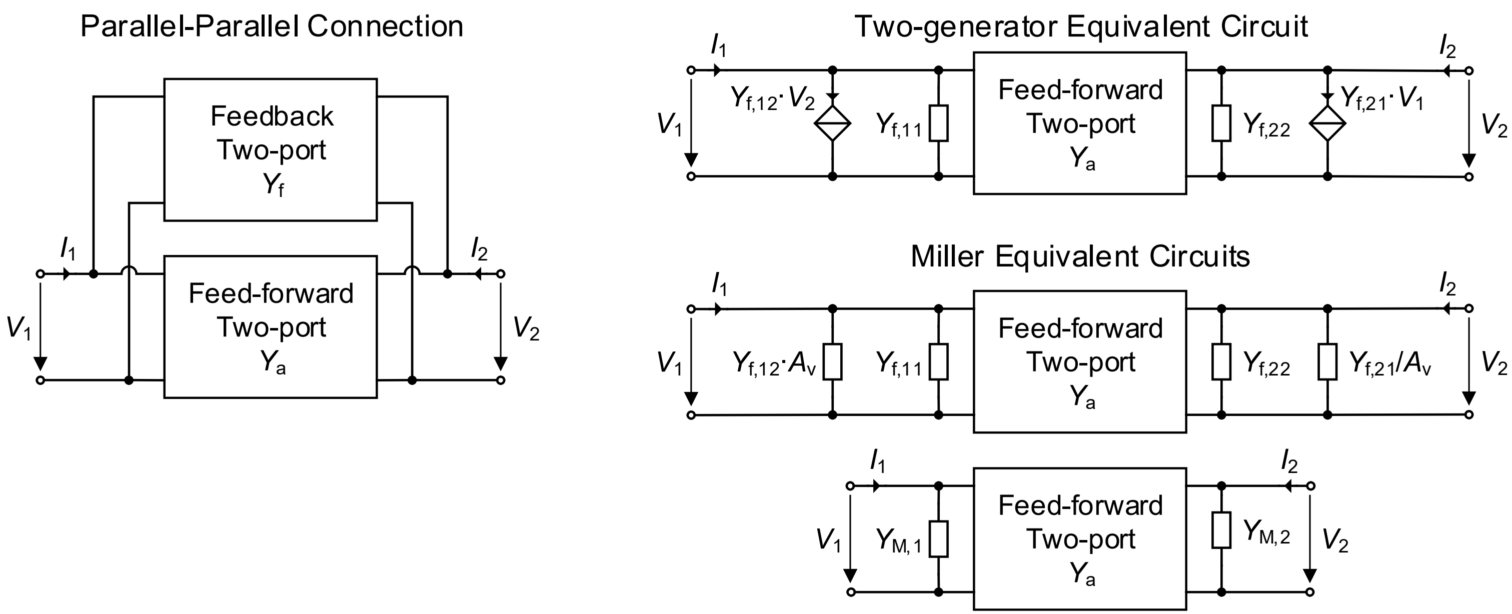
- **Appendices**

The Miller Theorem and Circuit Equivalence



- The feedback network can be embedded into the feed-forward network using the two-generator equivalent circuit
- The VCCSs can be replaced by the substitution theorem leading to the Miller equivalent circuits with the Miller admittances given by

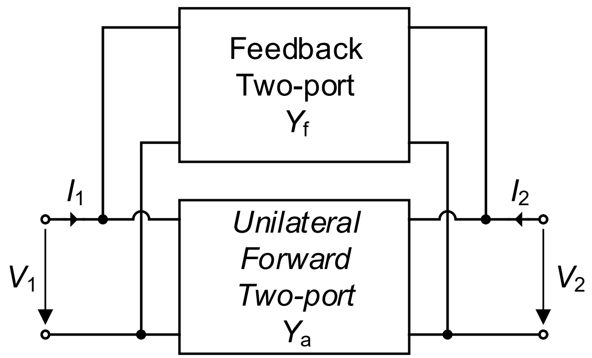
$$Y_{M,1} = Y_{f,11} + Y_{f,12} \cdot A_v \text{ and } Y_{M,2} = Y_{f,22} + \frac{Y_{f,21}}{A_v}$$

- where $A_v \triangleq V_2/V_1$ is the closed-loop voltage gain

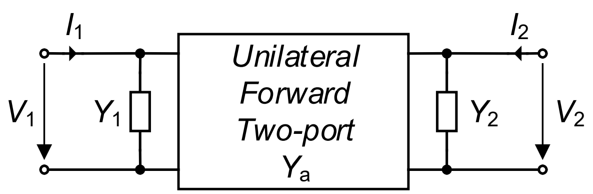
The Miller Theorem and Circuit Equivalence

- The problem is that we usually do not know the closed-loop voltage gain A_v a priori since it is what we are looking for
- So the Miller equivalent circuit only simplifies the calculation of the closed-loop gain and other network parameters such as the input admittance if we can use a reasonable approximation for the voltage gain
- What is usually done is to approximate the closed-loop gain with an approximate expression such as the low-frequency open-loop gain
- The next slides will highlight what are the condition for this approximation to hold
- The Miller approximation is usually done assuming a unilateral feed-forward amplifier

The Miller Theorem and Approximation



Miller theorem



$$Y_a = \begin{bmatrix} Y_{a,11} & 0 \\ Y_{a,12} & Y_{a,22} \end{bmatrix} \qquad Y_f = \begin{bmatrix} Y_{f,11} & Y_{f,12} \\ Y_{f,21} & Y_{f,22} \end{bmatrix}$$

$$Y_{M,1} = Y_{f,11} + Y_{f,12} \cdot A_v$$
$$Y_{M,2} = Y_{f,22} + \frac{Y_{f,21}}{A_v}$$

- Since the two two-ports are connected in parallel, we have

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{a,11} + Y_{f,11} & Y_{f,12} \\ Y_{a,21} + Y_{f,21} & Y_{a,22} + Y_{f,22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

- The resulting forward voltage gain A_v is then given by

$$A_v \triangleq \left. \frac{V_2}{V_1} \right|_{I_2=0} = -\frac{Y_{a,21} + Y_{f,21}}{Y_{a,22} + Y_{f,22}}$$

The Miller Theorem and Approximation

- The input admittance Y_{in} is given by

$$Y_{in} \triangleq \left.\frac{I_1}{V_1}\right|_{I_2=0} = Y_{a,11} + Y_{f,11} - Y_{f,12}\frac{Y_{a,21} + Y_{f,21}}{Y_{a,22} + Y_{f,22}} = Y_{a,11} + Y_{f,11} + Y_{f,12}A_v$$

- and output admittance Y_{out} is given by

$$Y_{out} \triangleq \left.\frac{I_2}{V_2}\right|_{I_1=0} = Y_{a,22} + Y_{f,22} - Y_{f,12}\frac{Y_{a,21} + Y_{f,21}}{Y_{a,11} + Y_{f,11}}$$

- Applying the Miller theorem results in the following relation for the Miller equivalent two-port

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{a,11} + Y_{f,11} + Y_{f,12}A_v & 0 \\ Y_{a,21} & Y_{a,22} + Y_{f,22} + \dfrac{Y_{f,21}}{A_v} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

- It can be seen that Miller's theorem does not take into account the bilateral characteristic of the circuit (i.e. the Miller equivalent two-port remains unilateral which is not the case of the original two-port even if Y_a is assumed unilateral)

The Miller Theorem and Approximation

- The forward gain $A_{v,M}$, the input admittance $Y_{in,M}$ and the output admittance $Y_{out,M}$ of the Miller equivalent network can be obtained as

$$A_{v,M} \triangleq \left.\frac{V_2}{V_1}\right|_{I_2=0} = -\frac{Y_{M,21}}{Y_{M,22}} = -\frac{Y_{a,21} + Y_{f,21}}{Y_{a,22} + Y_{f,22}}$$

$$Y_{in,M} \triangleq \left.\frac{I_1}{V_1}\right|_{I_2=0} = Y_{a,11} + Y_{f,11} + Y_{f,12} A_v$$

$$Y_{out,M} \triangleq \left.\frac{I_2}{V_2}\right|_{I_1=0} = Y_{a,22} + Y_{f,22} + \frac{Y_{f,21}}{A_v}$$

- Comparing these results to the one of the original network show that the Miller theorem provides a means of calculating the forward voltage gain and the input admittance in an exact manner
- However, the output admittance is not correctly calculated because the input admittance $Y_{a,11}$ is not taken into account in the output admittance

The Miller Theorem and Approximation

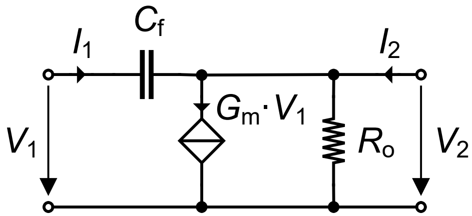
- To make the application of the Miller theorem simple it is often assumed that the closed-loop voltage gain magnitude $|A_v|$ (i.e. with the feedback network) is about equal to the open-loop voltage gain magnitude $|A_{v0}|$

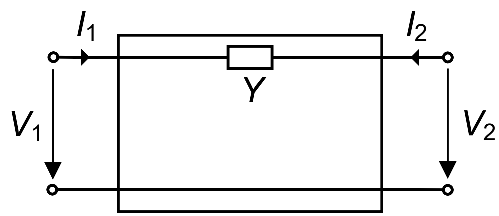
$$|A_v| \cong |A_{v0}| = \left|-\frac{Y_{a,21}}{Y_{a,22}}\right|$$

- This is the case when $|Y_{a,21}| \gg |Y_{f,21}|$ and $|Y_{a,22}| \gg |Y_{f,22}|$
- The above conditions just mean that the feedback network does not load the output of the feedforward network
- The input admittance can then be approximated using the open-loop gain without calculating the closed-loop gain

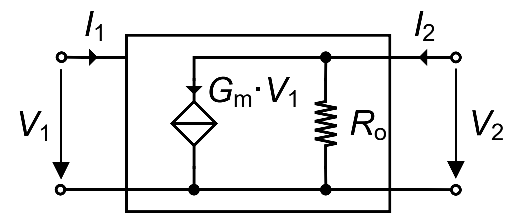
$$Y_{in,M} \cong Y_{a,11} + Y_{f,11} - Y_{f,12}\,\frac{Y_{a,21}}{Y_{a,22}}$$

Example





$$Y_f = \begin{bmatrix} Y & -Y \\ -Y & Y \end{bmatrix}$$



$$Y_a = \begin{bmatrix} 0 & 0 \\ G_m & G_o \end{bmatrix}$$

- The voltage gain is approximated by the dc gain

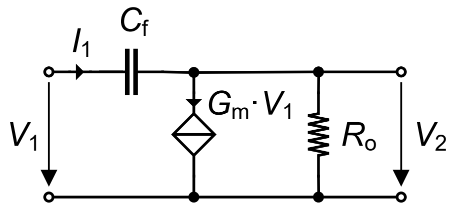
$$A_v \cong -\frac{Y_{a,21}}{Y_{a,22}} = -G_m R_o$$

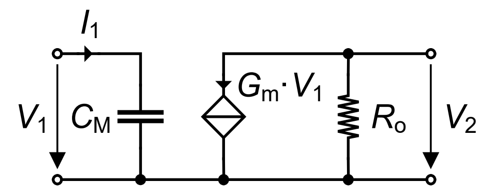
- The input admittance can then be approximated by

$$Y_{in} \cong sC_f + sC_f G_m R_o = sC_f \cdot (1 + G_m R_o)$$

- The above approximations are valid for $G_m \gg \omega C_f$ and $1/R_o \gg \omega C_f$

The Miller Capacitance





Miller capacitance:

$$C_M = (1 + G_m \cdot R_o) \cdot C_f \cong G_m \cdot R_o \cdot C_f$$

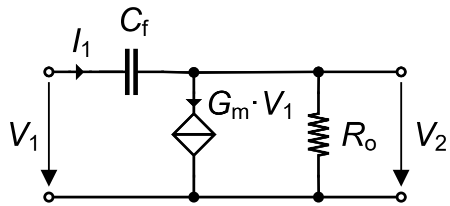
- The transfer function of the left circuit is given by

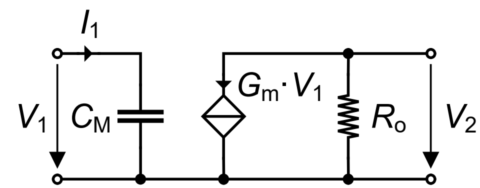
$$A_v(s) \triangleq \frac{V_2}{V_1} = -G_m \cdot R_o \cdot \frac{1 - C_f/G_m \cdot s}{1 + R_o C_f \cdot s}$$

- which includes a RHP zero at G_m/C_f
- Usually the dc voltage gain $G_m \cdot R_o \gg 1$. For $\omega \ll 1/(R_o C_f)$ and hence $\omega \ll 1/(R_o C_f) \ll G_m/C_f$, the voltage gain is approximately equal to the dc voltage gain

$$A_v \cong -G_m \cdot R_o$$

The Miller Capacitance





Miller capacitance:

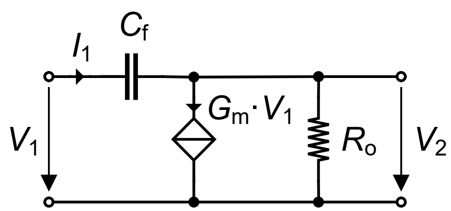
$$C_M = (1 + G_m \cdot R_o) \cdot C_f \cong G_m \cdot R_o \cdot C_f$$

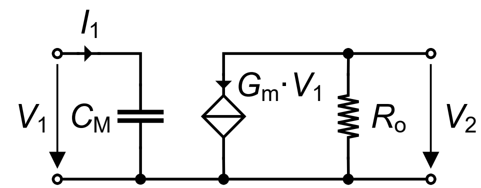
- The input admittance is given by

$$Y_{in} \triangleq \frac{I_1}{V_1} = \frac{(1 + G_m \cdot R_o) \cdot C_f \cdot s}{1 + R_o C_f \cdot s} \cong (1 + G_m \cdot R_o) \cdot C_f \cdot s = s \cdot C_M$$

- The input admittance is equal to the feedback capacitance C_f multiplied by $1 + G_m \cdot R_o \cong G_m \cdot R_o = |A_v|$, which the magnitude of the voltage gain
- This equivalent capacitance $C_M \triangleq (1 + G_m \cdot R_o) \cdot C_f \cong G_m \cdot R_o \cdot C_f$ is called the **Miller capacitance**

The Miller Approximation





Miller capacitance:

$$C_M = (1 + G_m \cdot R_o) \cdot C_f \cong G_m \cdot R_o \cdot C_f$$

- The left circuit can be approximated by the equivalent circuit shown on the right where there is no more coupling between input and output through the feedback capacitance
- The transfer function of the right circuit is simply given by
$$A_v = -G_m \cdot R_o$$
- The right half plane zero and the pole have disappeared but this gain corresponds to the gain of the left circuit for $\omega \ll 1/(R_o C_f)$ and assuming $G_m \cdot R_o \gg 1$
- The input admittance of the right circuit is the identical the one of the left circuit provided that $C_M = (1 + G_m \cdot R_o) \cdot C_f \cong G_m \cdot R_o \cdot C_f$