Fundamentals of Analog & Mixed Signal VLSI Design

Single-ended Differential Amplifier
Part 1

Christian Enz

Integrated Circuits Lab (ICLAB), Institute of Electrical and Micro-Engineering (IEM), School of Engineering (STI)

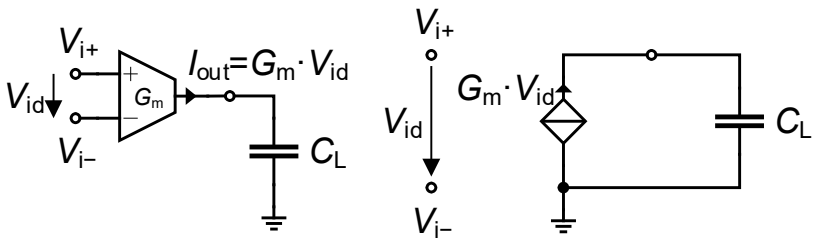
Swiss Federal Institute of Technology, Lausanne (EPFL), Switzerland

Outline

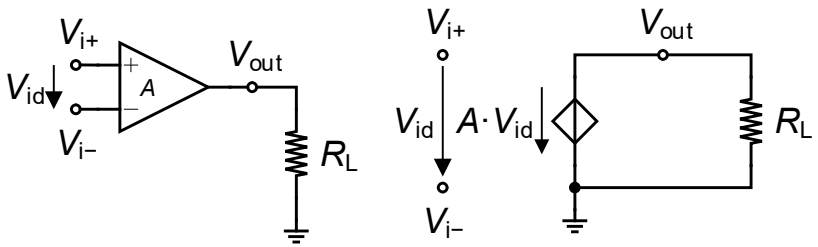
- **Introduction**
- OTA with capacitive feedback
- The single-stage or simple OTA
- The symmetrical OTA

Difference between OTA and OPAMP

OTA



OPAMP



- The OTA is ideally a differential transconductance amplifier modelled by a VCCS of value G_m
- It has a high output impedance and is therefore suited to drive high impedance loads such as capacitors
- Single-stage OTA have their dominant pole set by the load capacitance C_L

- The OPAMP is ideally a voltage amplifier which is modelled by a VCVS of value A
- It has a low output impedance and is therefore suited to drive low impedance loads such as resistances
- The dominant pole is set internally to the OPAMP by a compensation capacitor

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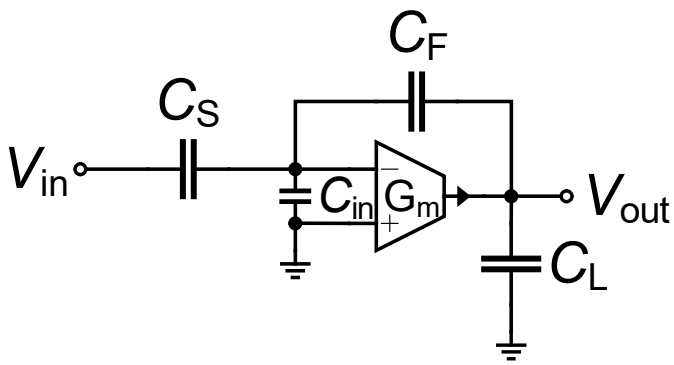
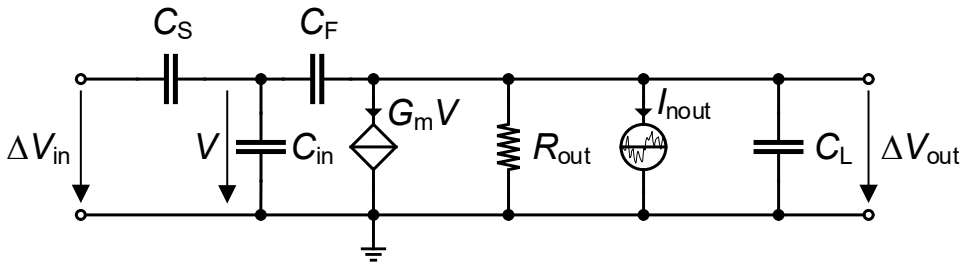
OTA with Capacitive Feedback



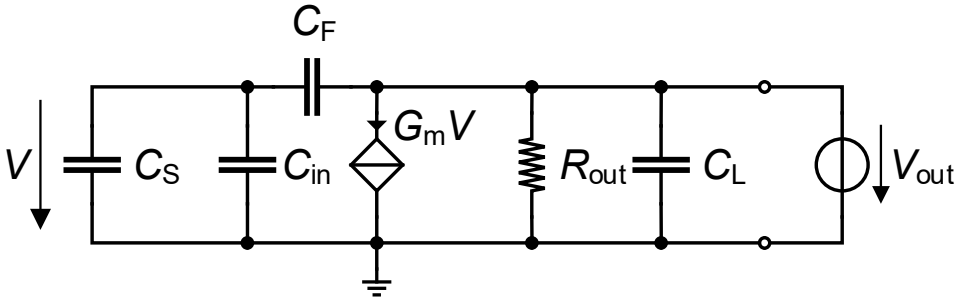


- OTAs are often appearing with a capacitive feedback (for example in SC amplifiers or filters) as shown above
- Assuming first that $C_{in} \ll C_S$, the voltage gain of the SC amplifier is set by the ratio

$$A_{v,ideal} = -\frac{C_S}{C_F}$$

- However, the input capacitance cannot really be neglected particularly in the case the input differential pair is biased in weak inversion leading to large input transistors

Feedback Gain and Total Load Capacitance



- The **feedback gain** β is given by

$$\beta \triangleq \frac{V}{V_{out}} = \frac{C_F}{C_F + C_S + C_{in}} = \frac{1}{1 + \alpha + \alpha_{in}}$$

- where $\alpha \triangleq \frac{C_S}{C_F} = \left|A_{v,ideal}\right|$ and $\alpha_{in} \triangleq \frac{C_{in}}{C_F}$
- The total equivalent capacitance at the OTA output is then given by

$$C_{out} = C_L + (1 - \beta) \cdot C_F = C_L + \frac{C_S + C_{in}}{C_F + C_S + C_{in}} \cdot C_F$$

$$= C_L + \beta \cdot (\alpha + \alpha_{in}) \cdot C_F = C_L + \frac{\alpha + \alpha_{in}}{1 + \alpha + \alpha_{in}} \cdot C_F$$

Closed-loop Transfer Function

- Modeling the OTA as a VCCS having a transconductance G_m with an output resistance R_{out}, the **closed-loop voltage gain** of the SC amplifier is given by

$$A_v(s) \triangleq \frac{V_{out}}{V_{in}} = A_0 \cdot \frac{1 - s/\omega_z}{1 + s/\omega_p} = A_0 \cdot \frac{1 - s \cdot \tau_z}{1 + s \cdot \tau_p}$$

- where

$$A_0 = -\alpha \cdot \frac{\beta \cdot A_{dc}}{1+\beta \cdot A_{dc}} \cong -\alpha = -\frac{C_S}{C_F} = A_{v,ideal} \text{ for } \beta \cdot A_{dc} \gg 1$$

$$\omega_p = \frac{1}{\tau_p} = \frac{1 + \beta \cdot A_{dc}}{R_{out} \cdot C_{out}} \cong \frac{\beta \cdot A_{dc}}{R_{out} \cdot C_{out}} = \frac{\beta \cdot G_m}{C_{out}} = \beta \cdot \omega_u$$

$$\omega_z = \frac{1}{\tau_z} = \frac{G_m}{C_F}$$

- with $A_{dc} = G_m R_{out}$ being the OTA **DC gain**, $\beta \cdot A_{dc}$ the **DC loop gain** and $\omega_u \cong G_m/C_{out}$ the **unity gain frequency** or **gain-bandwidth product**

Minimum Bias Current for Given Bandwidth

- The amplifier bandwidth is given by $\omega_p = \beta \cdot G_m / C_{out}$ where C_{out} is the total load capacitance which depends on the input capacitance C_{in} according

$$C_{out} = C_L + (1-\beta) \cdot C_F = C_L + \frac{C_S + C_{in}}{C_F + C_S + C_{in}} \cdot C_F$$

- When optimizing the OTA for low current consumption, the differential pair is often biased in moderate or even weak inversion leading to large transistors and therefore an increased input and output capacitance
- If we assume that the transistor parasitic capacitance at the drain is much smaller than the load capacitance, we can model this input capacitance as

$$C_{in} = W \cdot C_{GW}$$

- Where C_{GW} is the gate capacitance per unit width

Minimum Bias Current for Given Bandwidth

- Is there a minimum current for achieving a given DC gain and bandwidth ω_p?
- To answer this question we need to solve the following set of equations

$$\omega_p = \beta \cdot \frac{G_m}{C_{out}}$$
$$C_{out} = C_L + (1-\beta) \cdot C_F$$
$$\beta = \frac{C_F}{C_F + C_S + C_{in}}$$
$$C_{in} = C_{GW} \cdot W$$
$$I_b = I_{spec\square} \cdot \frac{W}{L} \cdot IC$$
$$G_m = \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC)$$

- for I_b and W (or W/L) for a given length L
- This leads to exactly the same equations used in the CS optimization but with different normalization

$$i_b \triangleq \frac{I_b}{I_{spec\square}} \cdot \frac{1}{\Omega} = \frac{IC}{g_{ms-\Theta}} \text{ and } AR \triangleq \frac{W}{L} \cdot \frac{1}{\Omega} = \frac{1}{g_{ms-\Theta}}$$

- where

$$\Omega \triangleq \frac{\omega_p}{\omega_L},\ \omega_L \triangleq \frac{I_{spec\square}}{\left(1+\frac{C_S}{C_L}+\frac{C_S}{C_F}\right) C_L\, nU_T},\ \omega_W \triangleq \frac{I_{spec\square}}{\left(1+\frac{C_L}{C_F}\right) C_{GW} L\, nU_T},\ \Theta \triangleq \frac{\omega_p}{\omega_W}$$

Optimum IC for Minimum Bias Current (without VS)

- The **optimum** IC, without VS, for which the bias current is minimum is given by

$$IC_{opt} = \left(\sqrt{\Theta \cdot (1+\Theta)} + \Theta + \frac{1}{2}\right)^2 - \frac{1}{4} =$$

$$= 2\Theta \cdot (1+\Theta) + (1+2\Theta) \cdot \sqrt{\Theta \cdot (1+\Theta)} \cong 2\Theta + \sqrt{\Theta} \text{ since } \Theta \ll 1$$

- There is a minimum IC below which the specified gain-bandwidth ω_u can no more be achieved (assuming no VS)

$$IC_{lim} = \Theta \cdot (1+\Theta) \cong \Theta$$

- This value corresponds to the vertical lines in the previous plot
- The optimum i_b and AR are given by

$$i_{bopt} \triangleq i_b(IC_{opt}) = 1 + 2\Theta + 2\sqrt{\Theta \cdot (1+\Theta)}$$

$$AR_{opt} \triangleq AR(IC_{opt}) = \frac{1}{\sqrt{\Theta \cdot (1+\Theta)}}$$

- IC_{opt}, i_{bopt} and AR_{opt} are plotted versus Θ in the next slide

Small-signal Step Response

- The small-signal step response is given by the inverse Laplace transform of $\Delta V_{out}(s) = \Delta V_{in}/s \cdot A_v(s)$, resulting in

$$\Delta V_{out}(t) = \Delta V_{in} \cdot A_0 \cdot \left[1 - \left(1 + \frac{\tau_z}{\tau_p}\right) \cdot e^{-\frac{t}{\tau_p}}\right]$$

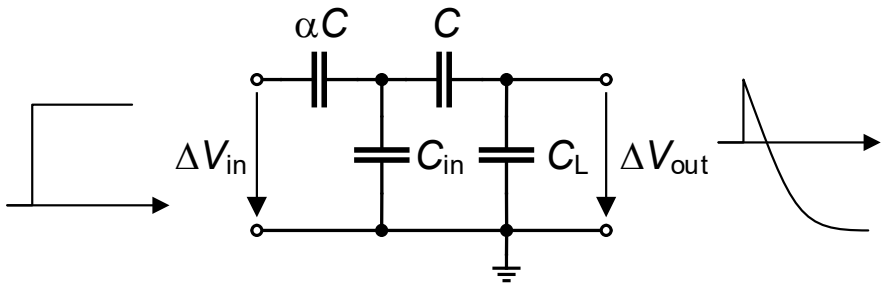
- As expected, the final value $\Delta V_{out}(t \to \infty)$ is given by

$$\Delta V_{out}(t \to \infty) = \Delta V_{in} \cdot A_0 = -\alpha \cdot \frac{\beta \cdot A_{dc}}{1 + \beta \cdot A_{dc}} \cdot \Delta V_{in} = \frac{-\alpha}{1 + \frac{1}{\beta \cdot A_{dc}}} \cdot \Delta V_{in}$$

$$\cong -\alpha \cdot (1 - \varepsilon_{gain}) \cdot \Delta V_{in} = -\alpha \cdot \Delta V_{in} \text{ for } \beta \cdot A_{dc} \gg 1$$

- where the OTA finite gain introduces a settling error $\varepsilon_{gain} = 1/(\beta \cdot A_{dc})$

Small-signal Step Response



circuit at time $t = 0^+$

- The positive zero introduces a step at $t = 0$ opposite to the final value

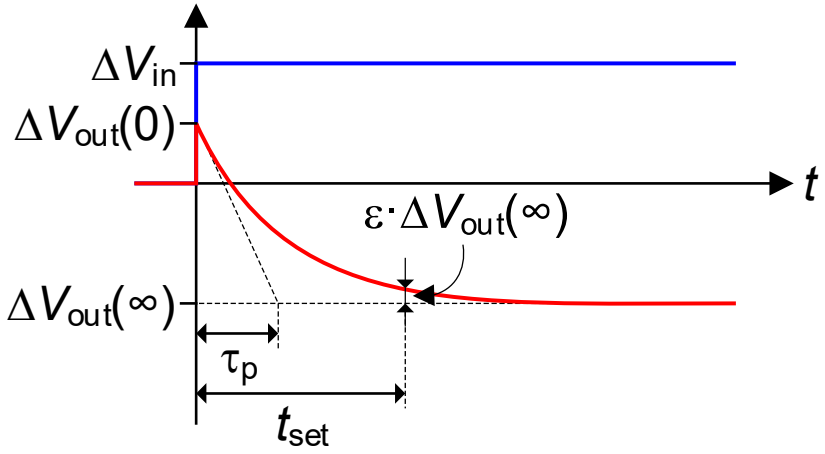
$$-\Delta V_{in} \cdot A_0 \cdot \frac{\tau_z}{\tau_p} \cong \Delta V_{in} \cdot \alpha \cdot \beta \cdot \frac{C}{C_{out}} = \Delta V_{in} \cdot \frac{\alpha}{(\alpha + \alpha_{in})(1 + \alpha_L) + \alpha_L}$$

- where $\alpha_L \triangleq C_L / C$
- This comes from the fact that at time $t = 0^+$, the OTA did not yet react and the voltage step ΔV_{in} imposed at the input is transmitted directly to the output through the capacitive network shown above, resulting in

$$\Delta V_{out}(0^+) = \Delta V_{in} \cdot \frac{\alpha C}{\alpha C + C_{in} + \frac{C \cdot C_L}{C + C_L}} \cdot \frac{C}{C + C_L} = \Delta V_{in} \cdot \frac{\alpha}{(\alpha + \alpha_{in})(1 + \alpha_L) + \alpha_L}$$

- which is identical to the expression above

Small-signal Settling Time



- The settling time t_{set} is defined as the time required to approach the equilibrium with a precision equal to ε

$$\Delta V_{out}(t = t_{set}) = (1 - \varepsilon) \cdot \Delta V_{out}(t \to \infty)$$

- which leads to

$$t_{set} = -\tau_p \cdot \ln\left(\frac{\varepsilon}{1 + \tau_z/\tau_p}\right) \cong -\tau_p \cdot \ln\left[\varepsilon \cdot \left(1 - \beta \cdot \frac{C}{C_{out}}\right)\right]$$

Large-signal Analysis – Slew-rate

- The above analysis was based on a **linear model** of the OTA
- However, at $t = 0^+$, the virtual ground may see a rather large voltage that will saturate the input differential pair
- In this situation, the current delivered by the OTA is limited by the differential pair bias current $2I_b$ and the output voltage is **slewing linearly** until the OTA input voltage comes back to the linear region
- This phenomena is described by the **slew-rate SR**, which is defined as the maximum change rate of the output voltage

$$SR = \frac{dV_{out}}{dt} = \frac{2I_b}{C_{out}}$$

- This slewing might significantly increase the settling time compared to the value obtained from the linear analysis
- In the following slides we will make a large-signal analysis and derive an expression of the settling time that includes the effect of slewing

Step Response including Slewing

- A large-signal analysis of the response to a negative input step $-\Delta V_{in}$ accounting for slewing can be performed assuming the differential pair is biased in WI
- It leads to the expression of the output voltage $V_{out}(t)$ normalized to the final value $V_{out\infty} = (\beta - 1)/\beta \cdot \Delta V_{in}$ given by

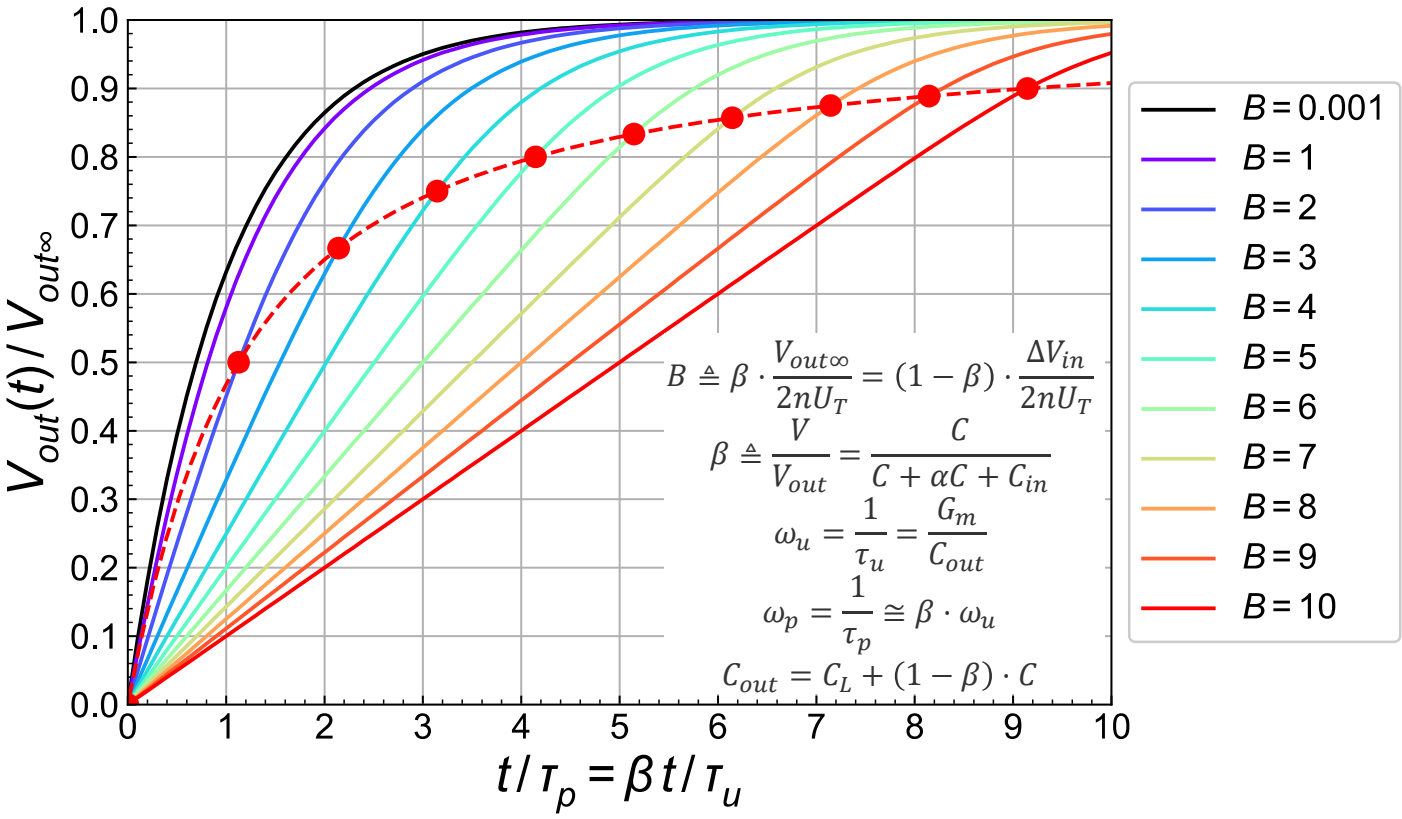
$$v_{out}(t) \triangleq \frac{V_{out}(t)}{V_{out\infty}} = 1 - \frac{1}{B} \cdot \ln\left(y(t) + \sqrt{y(t)^2 + 1}\right)$$

- with $y(t) \triangleq \sinh\left(\beta \cdot \frac{\Delta V_{out}}{2nU_T}\right) \cdot e^{-\frac{t}{\tau_p}}$ and where $\Delta V_{out} \triangleq V_{out\infty} - V_{out0}$ is the step at the output after the output voltage has settled and $V_{out0} \triangleq V_{out}(t = 0)$ is the initial value
- Parameter B is defined as

$$B \triangleq \beta \cdot \frac{V_{out\infty}}{2nU_T} = (1 - \beta) \cdot \frac{\Delta V_{in}}{2nU_T}$$

- The normalized output voltage has been plotted versus the normalized time t/τ_p for various values of the parameter B ranging from 0.1 (linear settling) to 10 (strongly nonlinear settling with slewing period dominating), assuming that $V_{out0} = 0$ and hence that $\Delta V_{out} = V_{out\infty}$

Step Response including Slewing



- The dot on each curve shows the point at which the slewing stops and the differential pair leaves saturation
- The above plot shows that the slewing time can be much larger than the linear settling time

Settling Time including Slewing

- The corresponding settling time (including the slewing period) is then given by

$$t_{set} = \tau_p \cdot \ln\left[\frac{\sinh\left(\beta \cdot \frac{\Delta V_{out}}{2nU_T}\right)}{\sinh(B \cdot \varepsilon)}\right] \cong \tau_p \cdot \ln\left[\frac{\sinh(B)}{\sinh(B \cdot \varepsilon)}\right]$$

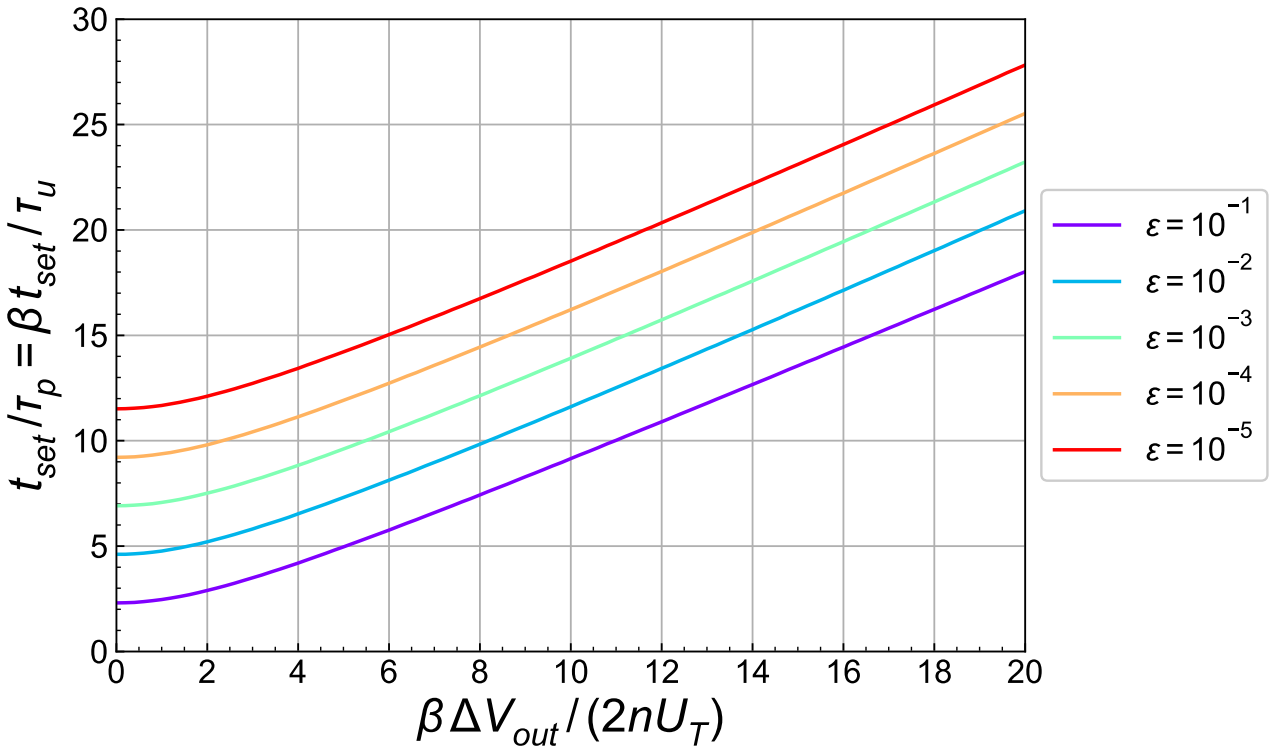
- since usually $V_{out0} \ll V_{out\infty}$ and therefore $\Delta V_{out} \cong V_{out\infty}$ resulting in

$$\beta \cdot \frac{\Delta V_{out}}{2nU_T} \cong \beta \cdot \frac{V_{out\infty}}{2nU_T} = B$$

- The settling time given by the above expression is plotted in the next slide versus parameter $B = \beta \cdot V_{out\infty}/(2nU_T)$ for various values of the targeted precision
- Note that for $\beta \cdot \Delta V_{out}/(2nU_T) \ll 1$, we find the small-signal settling time

$$t_{set} = \tau_p \cdot \ln\left(\frac{1}{\varepsilon}\right)$$

Settling Time including Slewing



$$\beta \cdot \frac{\Delta V_{out}}{2nU_T} \cong \beta \cdot \frac{V_{out\infty}}{2nU_T} = B$$

$$B \triangleq \beta \cdot \frac{V_{out\infty}}{2nU_T} = (1-\beta) \cdot \frac{\Delta V_{in}}{2nU_T}$$

$$\beta \triangleq \frac{V}{V_{out}} = \frac{C}{C + \alpha C + C_{in}}$$

$$\omega_u = \frac{1}{\tau_u} = \frac{G_m}{C_{out}}$$

$$\omega_p = \frac{1}{\tau_p} \cong \beta \cdot \omega_u$$

$$C_{out} = C_L + (1-\beta) \cdot C$$

- The value at the origin corresponds to the **small-signal settling time**
- The above plot shows that **slewing can significantly increase the settling time**
- This may be an issue in micropower SC circuits which can be circumvented by using inverter based OTA (which are class AB and hence are not limiting the current) or OTA with adaptive bias allowing for a much larger transient current

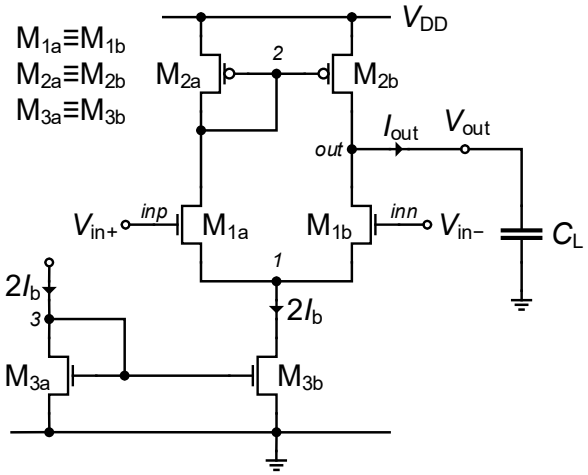
Example

- As an example we want to find the required bias current for the SC amplifier to achieve an unity voltage gain magnitude $A_0 = \alpha = 1$.
- Let's assume the SC amplifier works with two non-overlapping phases having a clock frequency $f_{ck} = 1\ MHz$
- Imposing that the amplifier needs to settle within a half clock period $t_{set} = T_s/2 = 500\ ns$ for an output step voltage $\Delta V_{out} = 1.2\ V$ with a settling error $\varepsilon = 10^{-3}$
- Choosing $\alpha C = C = 1\ pF$ and assuming the input and load capacitance are $C_{in} = 10\ fF$ and $C_L = 0.1\ fF$, respectively, we find that the output capacitance is $C_{out} = 602\ fF$, the feedback gain $\beta = 0.5$
- Assuming $n = 1.3$, we get $B = 9$ and $\tau_p = 38.5\ ns$ corresponding to $GBW = 8.3\ MHz$
- The required transconductance is then $G_m = 31.5\ \mu A/V$
- Assuming the differential pair is biased in WI, we get $I_b = 1\ \mu A$
- If we use the small-signal settling time formula we get $GBW = 4.4\ MHz$ and $I_b = 557\ nA$ which is almost half the value obtained from the large-signal settling estimation
- We see that if we use the simplest linear settling time estimation, we will not achieve the desired settling error

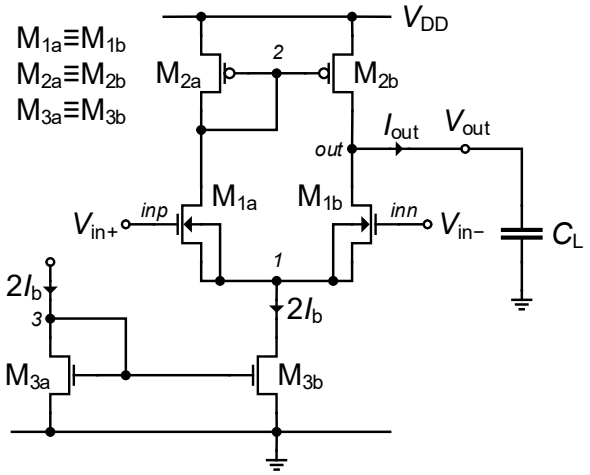
Outline

- Introduction
- Settling time of OTA with capacitive feedback
- **The simple OTA**
- The symmetrical OTA

The Simple Differential OTA



M_{1a}-M_{1b} in common substrate



M_{1a}-M_{1b} in separate well

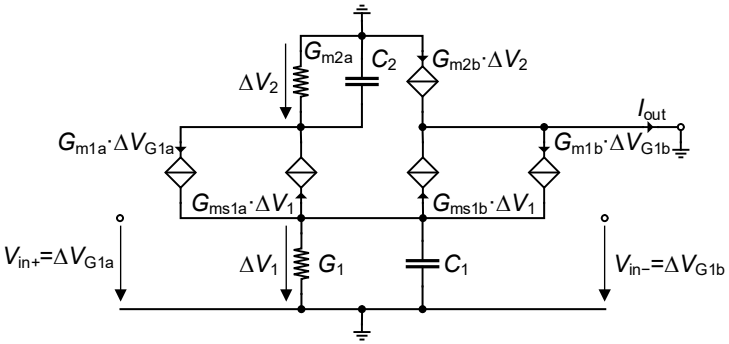
- Combination of a differential pair and a current mirror
- Differential and common-mode input voltages defined as

$$V_{id} \triangleq V_{in+} - V_{in-} \text{ and } V_{ic} \triangleq \frac{V_{in+}+V_{in-}}{2}$$

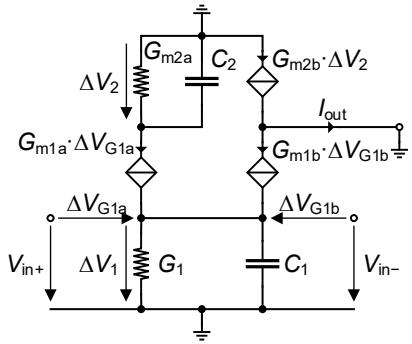
$$V_{in+} = V_{ic} + \frac{V_{id}}{2} \text{ and } V_{in-} = V_{ic} - \frac{V_{id}}{2}$$

- Differential- and common-mode defined by $V_{ic} = 0$ and $V_{id} = 0$, respectively

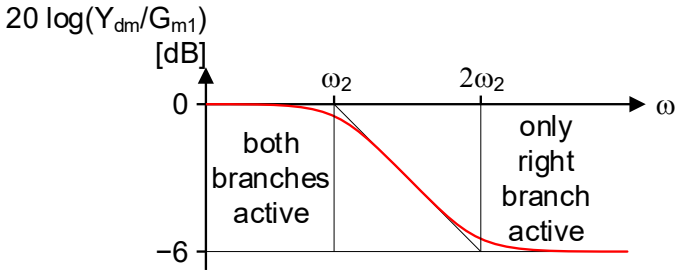
The Simple OTA – Differential Transadmittance



M_{1a}-M_{1b} in common substrate



M_{1a}-M_{1b} in separate well



- Small-signal circuit assuming that $G_{ds} \ll G_m < G_{ms}$ for all transistors
- Assuming also a perfect matching between the two current branches, i.e. $G_{m1a} = G_{m1b} = G_{m1}$, $G_{m2a} = G_{m2b} = G_{m2}$, in differential mode ($V_{ic} = 0$), $\Delta V_1 = 0$ and hence the effect of $G_{ms1a} = G_{ms1b} = G_{ms1}$ is null
- The differential transadmittance is then given by

$$Y_{md} \triangleq \frac{I_{out}}{V_{id}} = G_{m1} \cdot \frac{1 + s\,\frac{\tau_p}{2}}{1 + s\,\tau_p} = G_{m1} \cdot \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}}$$

- where $\tau_p = \frac{1}{\omega_p} = \frac{C_2}{G_{m2}}$ and $\omega_z = 2\omega_p$
- At dc the differential transconductance is simply equal to G_{m1}

The Simple OTA – Differential Voltage Gain

- The differential voltage gain A_{vd} is then given by

$$A_{dm} \triangleq \frac{V_{out}}{V_{id}} = \frac{Y_{md}}{Y_L} = Y_{md} \cdot Z_L \text{ with } Y_L = \frac{1}{Z_L} = G_o + sC_L$$

- where Y_L is the total output admittance with $G_o = G_{ds3} + G_{ds4}$, A_{vd} then writes

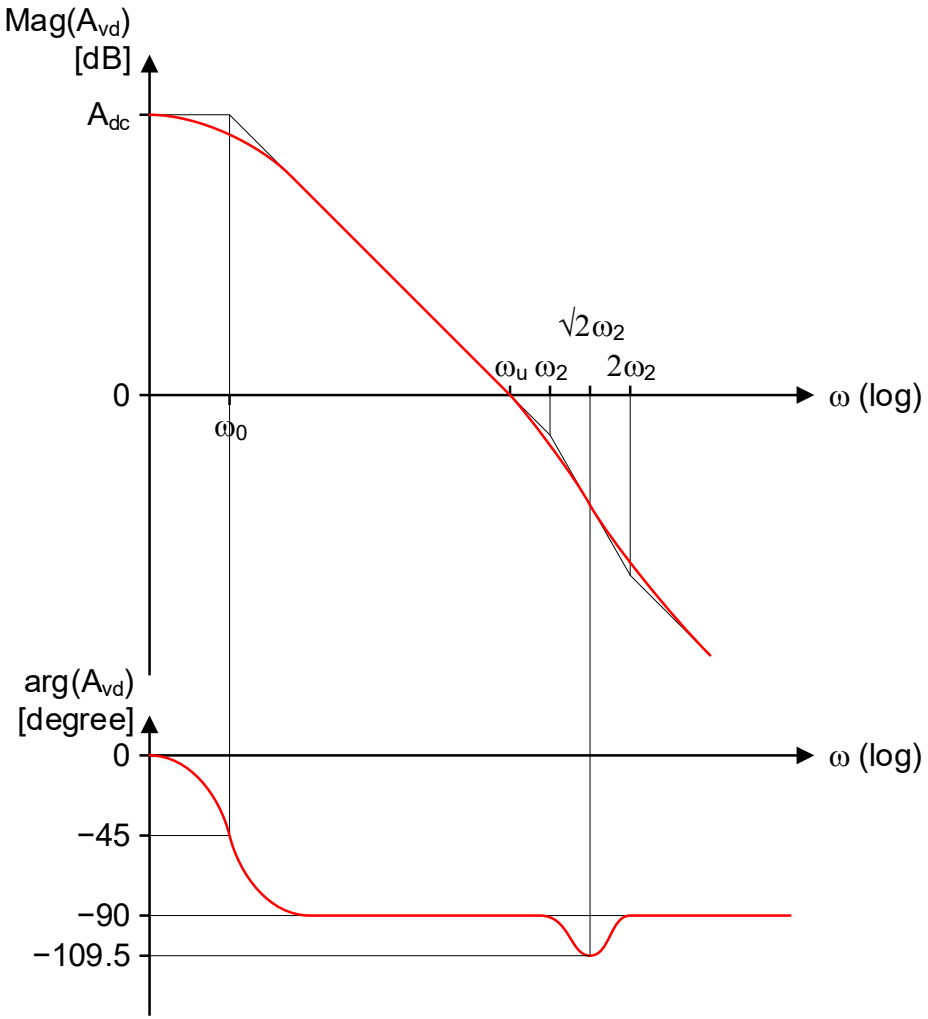
$$A_{dm} = \frac{G_{m1}}{G_o + sC_L} \cdot \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}} = A_{dc} \cdot \frac{1 + \frac{s}{\omega_z}}{\left(1 + \frac{s}{\omega_0}\right)\left(1 + \frac{s}{\omega_p}\right)}$$

- where

$$A_{dc} = \frac{G_{m1}}{G_o}, \omega_0 = \frac{G_o}{C_L}, \omega_p = \frac{G_{m2}}{C_2}, \omega_z = 2\omega_p$$

- ω_0 is the **dominant pole** since usually $G_o \ll G_{m2}$ and hence $\omega_0 \ll \omega_p$
- ω_p is the **non-dominant** pole
- The zero is equal to twice the non-dominant pole
- ω_p and $\omega_z = 2\omega_p$ form a **doublet**
- Since ω_p and ω_z are close they can be ignored in a 1st-order approximation

The Simple OTA – Bode Plots



$$A_{dm} = A_{dc} \cdot \frac{1 + \frac{s}{\omega_z}}{\left(1 + \frac{s}{\omega_0}\right)\left(1 + \frac{s}{\omega_p}\right)}$$

$$\cong \frac{A_{dc}}{1 + \frac{s}{\omega_0}} \cong \frac{\omega_u}{s}$$

$$A_{dc} = \frac{G_{m1}}{G_0}$$

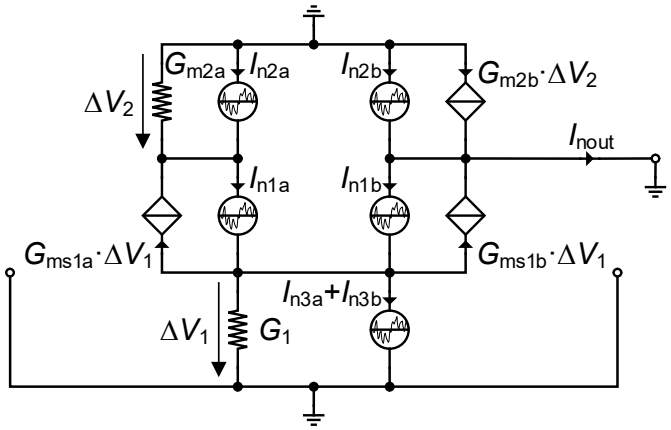
$$\omega_0 = \frac{G_0}{C_L}$$

$$\omega_p = \frac{G_{m2}}{C_2}$$

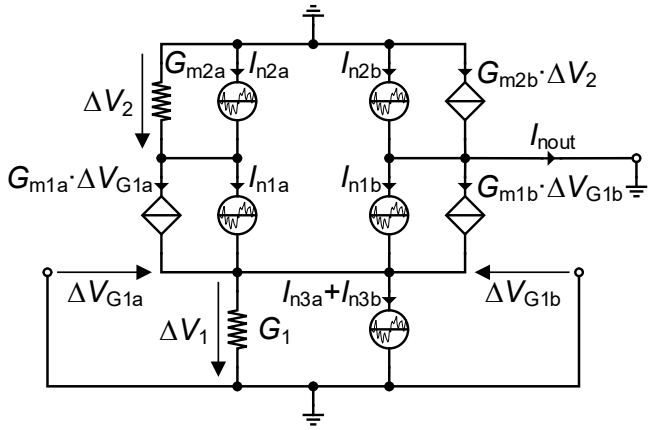
$$\omega_z = 2\omega_p$$

$$\omega_u = A_{dc} \cdot \omega_0 = \frac{G_{m1}}{C_L}$$

The Simple OTA – Noise Analysis



M_{1a}-M_{1b} in common substrate



M_{1a}-M_{1b} in separate well

$$\Delta V_{G1a} = \Delta V_{G1b} = -\Delta V_1$$

- The small-signal schematics for calculating the output noise current are shown above where all the output conductances have been neglected
- Assuming perfect matching (i.e. $G_{m1a} = G_{m1b} = G_{m1}$ and $G_{m2a} = G_{m2b} = G_{m2}$), the bottom currents sources I_{n3a} and I_{n3b} split equally between the two branches so that they do not produce any net current at the output
- It can be shown that the output noise current is simply given by

$$I_{nout} = I_{n1a} - I_{n1b} - I_{n2a} + I_{n2b}$$

The Simple OTA – Input-referred Noise Resistance

- Writing the output noise current PSD as $S_{nout}(f) = 4kTG_{nout}(f)$ with $G_{nout}(f) = G_{n1a}(f) + G_{n1b}(f) + G_{n2a}(f) + G_{n2b}(f) = 2\big(G_{n1}(f) + G_{n2}(f)\big)$
- where $G_{ni}(f) = \gamma_{ni}G_{mi} + G_{mi}^2 \frac{\rho_i}{W_i L_i f}$ for $i = 1,2$
- The noise can be referred to the differential input by dividing G_{nout} by G_{m1}, resulting in

$$R_{nin}(f) = \frac{G_{nout}(f)}{G_{m1}^2} = R_{nt} + R_{nf}(f)$$

- where R_{nt} is the part of the input-referred noise resistance corresponding to the thermal noise

$$R_{nt} = 2\left(\frac{\gamma_{n1}}{G_{m1}} + \gamma_{n2}\frac{G_{m2}}{G_{m1}^2}\right) = 2\frac{\gamma_{n1}}{G_{m1}}\left(1 + \frac{\gamma_{n2}}{\gamma_{n1}}\frac{G_{m2}}{G_{m1}}\right)$$

- and $R_{nf}(f)$ is the part corresponding to the 1/f noise

$$R_{nf}(f) = 2\left[\frac{\rho_n}{W_1 L_1 f} + \left(\frac{G_{m2}}{G_{m1}}\right)^2 \frac{\rho_p}{W_2 L_2 f}\right] = \frac{2\rho_n}{W_1 L_1 f}\left[1 + \left(\frac{G_{m2}}{G_{m1}}\right)^2 \frac{\rho_p}{\rho_n}\frac{W_1 L_1}{W_2 L_2}\right]$$

The Simple OTA – Thermal Noise Excess Factor

- In the same way a noise excess factor γ_n has been defined for a single transistor, a thermal noise excess factor can also be defined for the OTA as

$$\gamma_{ota} \triangleq G_m \cdot R_{nt} = 2\gamma_{n1} \cdot (1 + \eta_{th})$$

- where

$$\eta_{th} = \frac{\gamma_{n2}}{\gamma_{n1}} \frac{G_{m2}}{G_{m1}}$$

- represents the contribution to the input-referred thermal noise of the current mirror relative to the differential pair
- The minimum value of the OTA noise excess factor is equal to that of the differential pair only $\gamma_{ota} = 2\gamma_{n1}$
- To limit the contribution of the current mirror to a minimum, $G_{m2}/G_{m1} \ll 1$
- This is a similar condition than the one discussed above for minimizing the V_T mismatch of the current mirror to the input-referred offset voltage
- This can be done by biasing M_{1a}-M_{1b} in **weak inversion** and M_{2a}-M_{2b} in **strong inversion**, respectively, resulting in

$$\gamma_{ota} = 2\gamma_{n1}\left(1 + \frac{\gamma_{n2}}{\gamma_{n1}} \frac{2n_1 U_T}{V_{G2} - V_{T0p}}\right) = n_1\left(1 + \frac{8n_2}{3} \frac{U_T}{V_{G2} - V_{T0p}}\right)$$

The Simple OTA – Input-referred Flicker Noise

- The input-referred flicker noise resistance is given by

$$R_{nf}(f) = \frac{2\rho_n}{W_1 L_1 f} \cdot (1 + \eta_{fl})$$

- where

$$\eta_{fl} = \left(\frac{G_{m2}}{G_{m1}}\right)^2 \frac{\rho_p}{\rho_n} \frac{W_1 L_1}{W_2 L_2}$$

- represents the contribution to the input-referred flicker noise of the current mirror relative to the differential pair
- It depends on the ratio of the flicker noise parameters ρ_p/ρ_n and can be minimized by having a large G_{m2}/G_{m1} ratio and a large $W_1 L_1/(W_2 L_2)$ ratio

The Simple OTA – Flicker Noise Corner Frequency

- The 1/f noise corner frequency f_k is defined as the frequency at which the 1/f noise becomes equal to the thermal noise

$$R_{nf}(f_k) = R_{nt}$$

- which leads to

$$f_k = \frac{1}{R_{nt}} \frac{2\rho_n}{W_1 L_1} \cdot (1 + \eta_{fl}) = \frac{G_{m1}}{\gamma_{ota}} \cdot \frac{2\rho_n}{W_1 L_1} \cdot (1 + \eta_{fl})$$

- The transconductance G_{m1} is set by the constraints either on thermal noise or on bandwidth (GBW product)
- The corner frequency can be reduced by increasing $W_1 L_1$ and $W_2 L_2$ at the same time to conserve the same η_{fl} factor
- Assuming $(G_{m2}/G_{m1})^2 \ll 1$ as required by the constraints on minimizing the contribution of the current mirror to the input-referred offset and thermal noise the corner frequency is then mainly set by the differential pair transistor area

$$f_k \cong \frac{G_{m1}}{\gamma_{ota}} \cdot \frac{2\rho_n}{W_1 L_1}$$

The Simple OTA – Offset Voltage Analysis

- Mismatch between the two transistors of the differential pair M_{1a}-M_{1b} and of the current mirror M_{2a}-M_{2b} causes some current to flow at the output even for a zero differential input voltage $V_{id} = 0$
- This output current can be compensated by applying a certain differential input voltage defined as the input-referred offset voltage V_{os}
- The analysis of the mismatch effects for deriving the variance of the input-referred offset voltage can be done similarly to the noise analysis
- We can reuse the expression of the output noise current

$$I_{out} = I_{n1a} - I_{n1b} - I_{n2a} + I_{n2b}$$

- but with $I_{n1a} = +\Delta I_{D1}/2$, $I_{n1b} = -\Delta I_{D1}/2$, $I_{n2a} = -\Delta I_{D2}/2$ and $I_{n2b} = +\Delta I_{D2}/2$, where ΔI_{D1} and ΔI_{D2} are the current mismatch in the differential and current mirror, respectively
- The output current then simplifies to

$$I_{out} = \Delta I_{D1} + \Delta I_{D2}$$

The Simple OTA – Input-referred Offset Voltage

- Of course ΔI_{D1} and ΔI_{D2} are random variables and the variance of the output offset current is then given by

$$\sigma^2_{I_{out}} = \sigma^2_{\Delta I_{D1}} + \sigma^2_{\Delta I_{D2}} = I_b^2 \cdot \left(\sigma^2_{\Delta I_{D1}/I_{D1}} + \sigma^2_{\Delta I_{D2}/I_{D2}}\right)$$

- where $$\sigma^2_{\Delta I_{Di}/I_{Di}} = \sigma^2_{\beta_i} + \left(\frac{G_{mi}}{I_b}\right)^2 \sigma^2_{V_{Ti}} \text{ for } i = 1,2$$

- with $$\sigma^2_{\beta_i} = \frac{A^2_\beta}{W_i L_i} \text{ and } \sigma^2_{V_{Ti}} = \frac{A^2_{V_T}}{W_i L_i} \text{ for } i = 1,2$$

- The variance of the output offset current then becomes

$$\sigma^2_{I_{out}} = I_b^2 \cdot \left(\sigma^2_{\beta_1} + \sigma^2_{\beta_2}\right) + G^2_{m1} \cdot \sigma^2_{V_{T1}} + G^2_{m2} \cdot \sigma^2_{V_{T2}}$$

- The variance of the input-referred offset voltage is obtained by dividing the variance of the output offset current resulting in

$$\sigma^2_{V_{os}} = \left(\frac{I_b}{G_{m1}}\right)^2 \left(\sigma^2_{\beta_1} + \sigma^2_{\beta_2}\right) + \left(\frac{G_{m2}}{G_{m1}}\right)^2 \sigma^2_{V_{T2}} + \sigma^2_{V_{T1}}$$

The Simple OTA – Input-referred Offset Voltage

$$\sigma_{V_{os}}^2 = \left(\frac{I_b}{G_{m1}}\right)^2 \left(\sigma_{\beta_1}^2 + \sigma_{\beta_2}^2\right) + \left(\frac{G_{m2}}{G_{m1}}\right)^2 \sigma_{V_{T2}}^2 + \sigma_{V_{T1}}^2$$

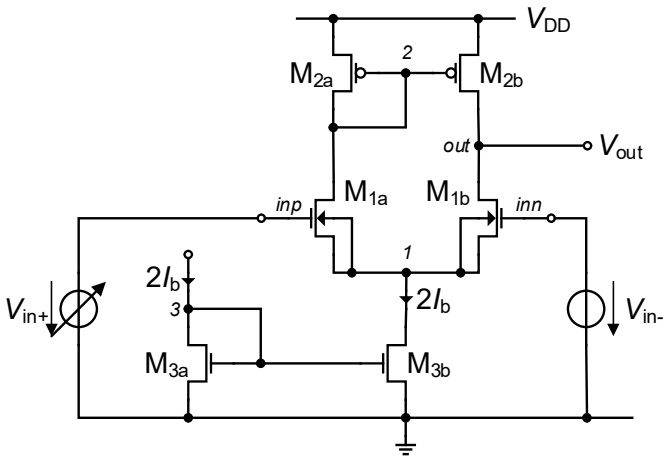
- We see that the contribution of the β mismatch to the input-referred offset voltage can be minimized by choosing I_b/G_{m1} as small as possible which can be done by biasing the transistors of the differential pair in **weak inversion**
- Secondly, the contribution of the V_T mismatch of the current mirror can also be minimized by setting $G_{m2}/G_{m1} \ll 1$
- Since M_{1a} and M_{2a} (M_{1b} and M_{2b}) share the same bias current $I_{D1} = I_{D2} = I_b$, this can only be done by biasing the current mirror in **strong inversion** and hence $G_{m1} = I_{D1}/(n_1 U_T)$ and $G_{m2} = 2I_{D2}/(n_2 V_{DSsat2})$ leading to

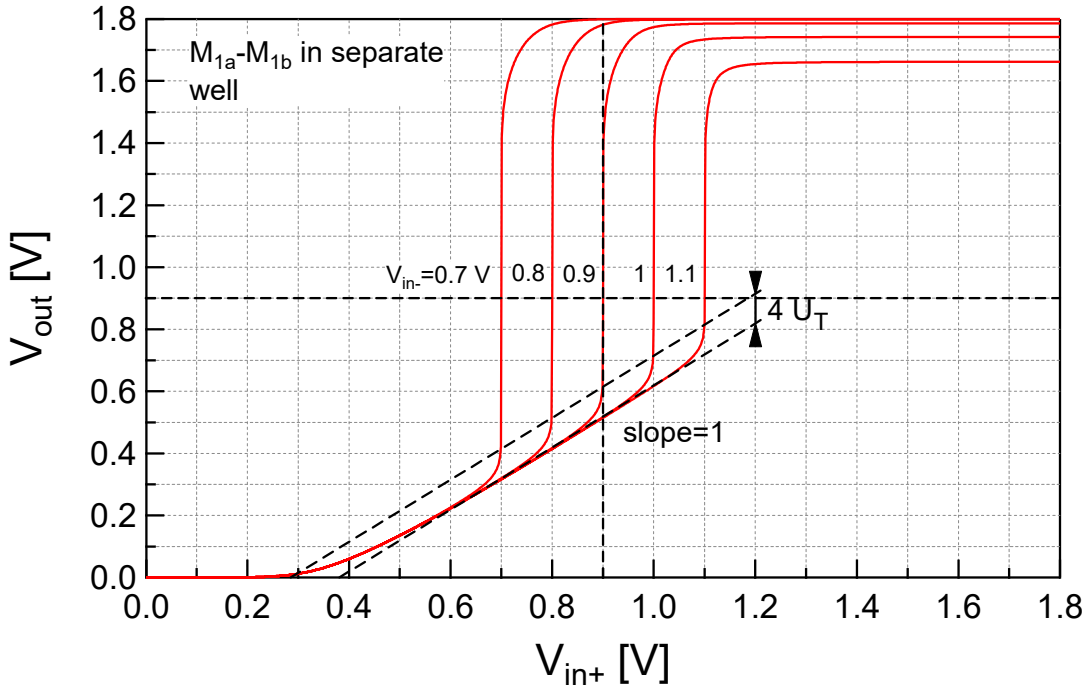
$$\frac{G_{m2}}{G_{m1}} = \frac{2n_1 U_T}{n_2 V_{DSsat2}} = \frac{2n_1 U_T}{n_2 V_{P2}} \cong \frac{2n_1 U_T}{V_{G2} - V_{T0p}} \ll 1$$

- The overdrive voltage of M_{2a}-M_{2b} $V_{G2} - V_{T0p}$ needs to be set as large as possible without pushing M_{1a} out of saturation

The Simple OTA – Large-signal Transfer Characteristic

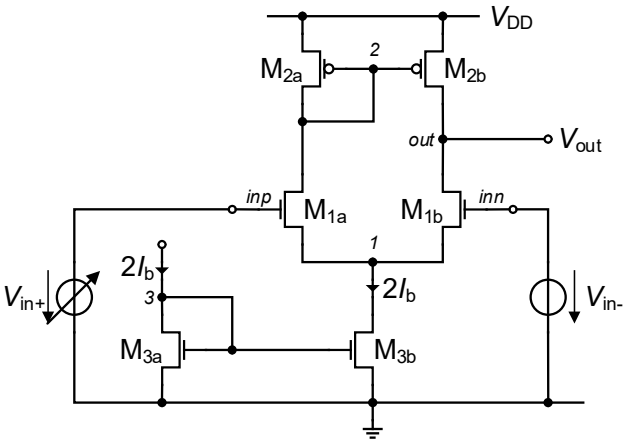
M_{1a}-M_{1b} in separate well

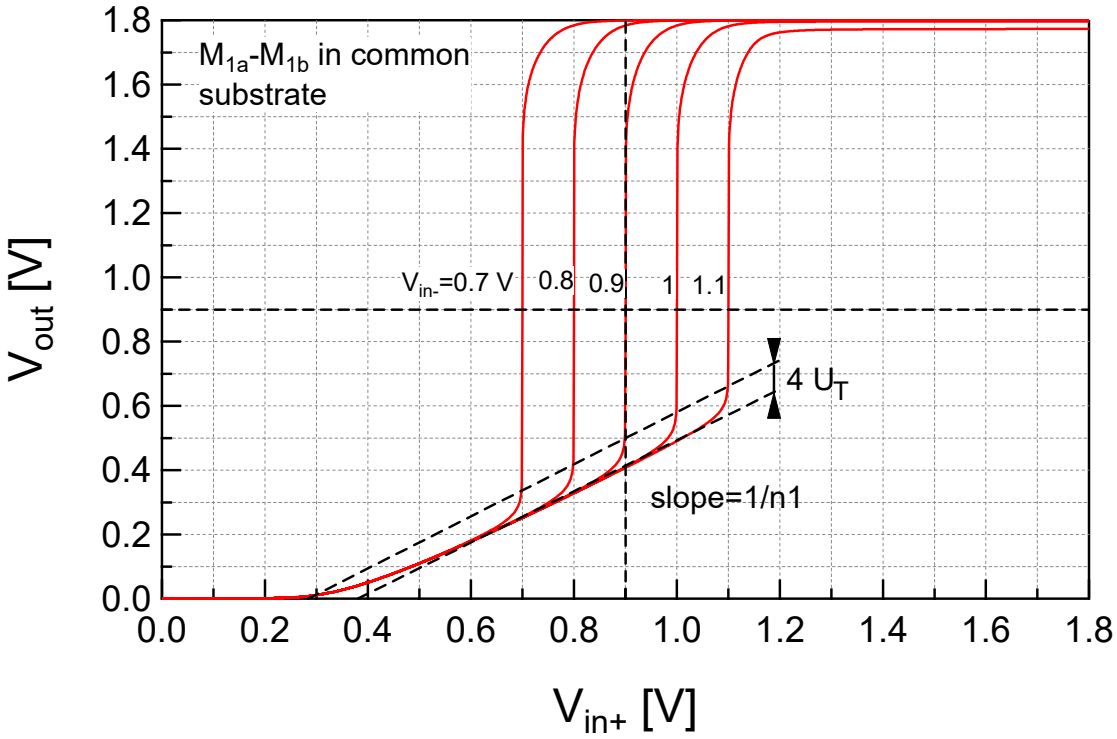




The Simple OTA – Large-signal Transfer Characteristic

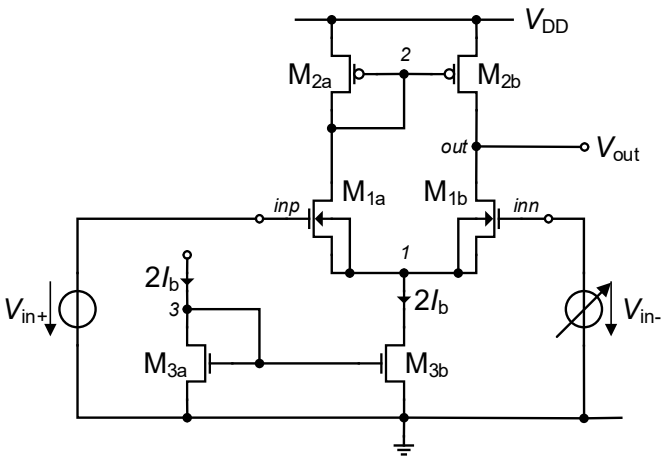
M_{1a}-M_{1b} in common substrate

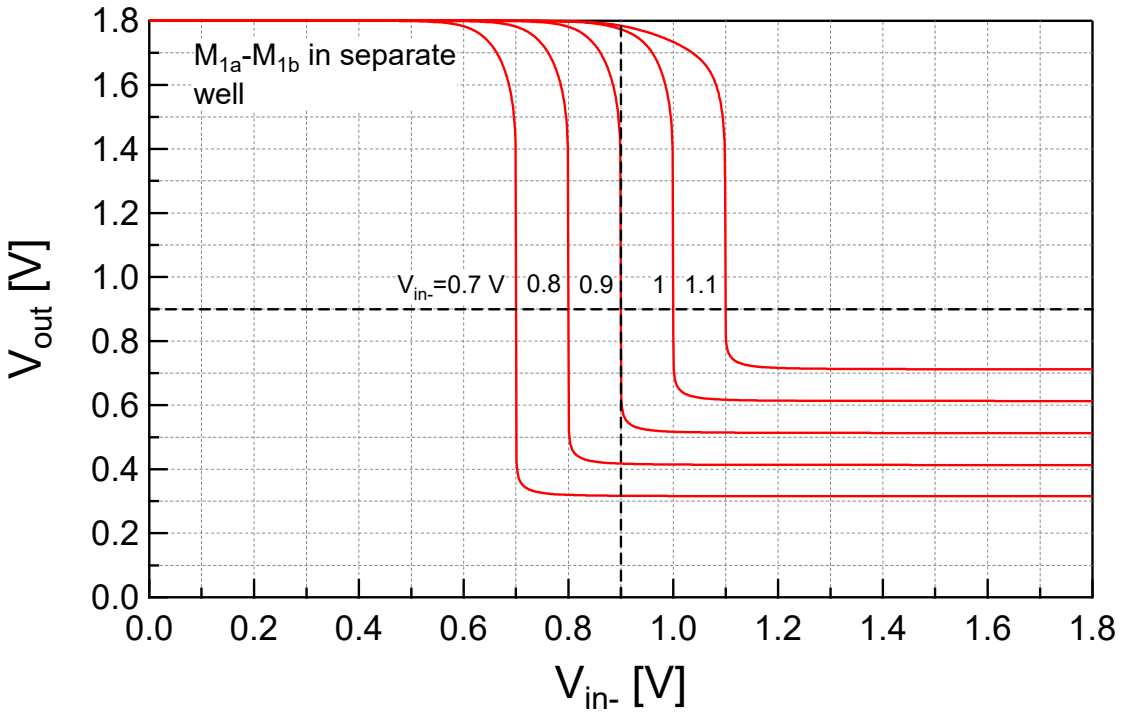




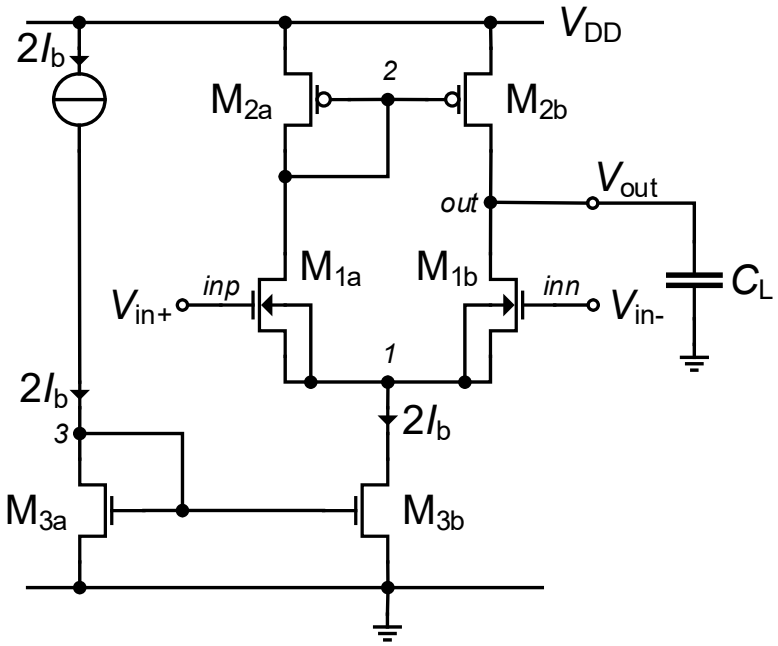
The Simple OTA – Large-signal Transfer Characteristic

M_{1a}-M_{1b} in separate well





The Simple OTA – Example



- Size a simple OTA for the following specifications

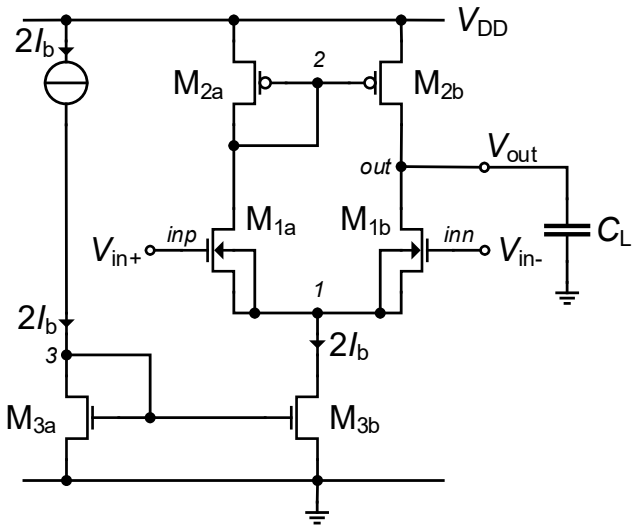
$$A_{dc} \geq 60\ dB, GBW \geq 1\ MHz, V_{os} \leq 10\ mV$$

- for a load capacitance $C_L = 1\ pF$ and for the process parameters corresponding to a 180nm CMOS process given in the next slide
- The design procedure is detailed in the corresponding Jupyter Notebook

Process Parameters

Parameter	N-channel	P-channel	Unit
C_{ox}	8.443		$\frac{fF}{\mu m^2}$
V_{T0}	0.455	0.457	V
$I_{spec\square}$	715	173	nA
n_0	1.27	1.3	-
λ	24	20	$\frac{V}{\mu m}$
A_{V_T}	5	5	$mV \cdot \mu m$
A_β	0.01	0.01	μm
ρ	0.058	0.483	$\frac{V \cdot m^2}{A \cdot s}$

Sizing Summary



Specifications

Name	Value
AdcdB	60
GBWmin	1.0E+6
CL	1E-12
VDD	1.8
Wmin	200.0E-9
Lmin	180.0E-9
Vosmax	10.0E-3
PMdeg	60

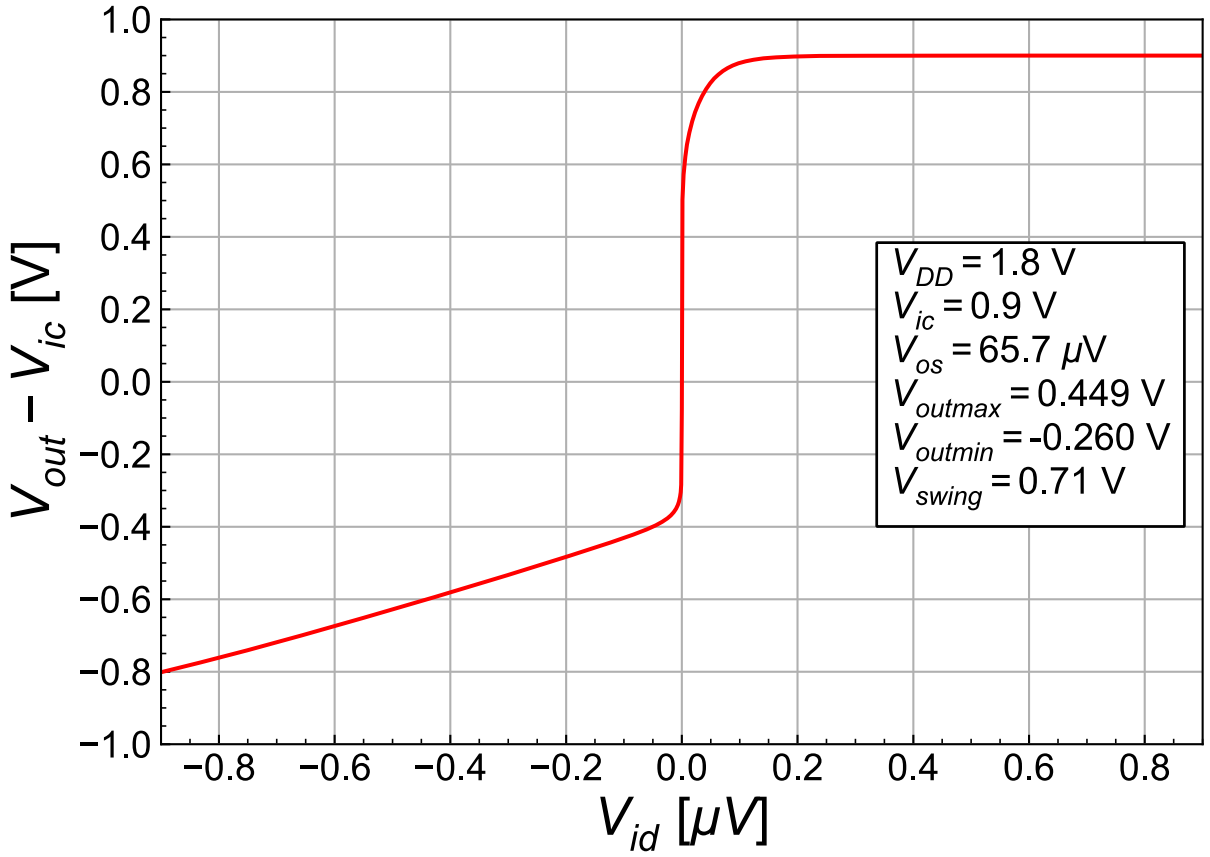
Bias

Name	Value
VDD	1.8
VSS	0
Ib	250.0E-9

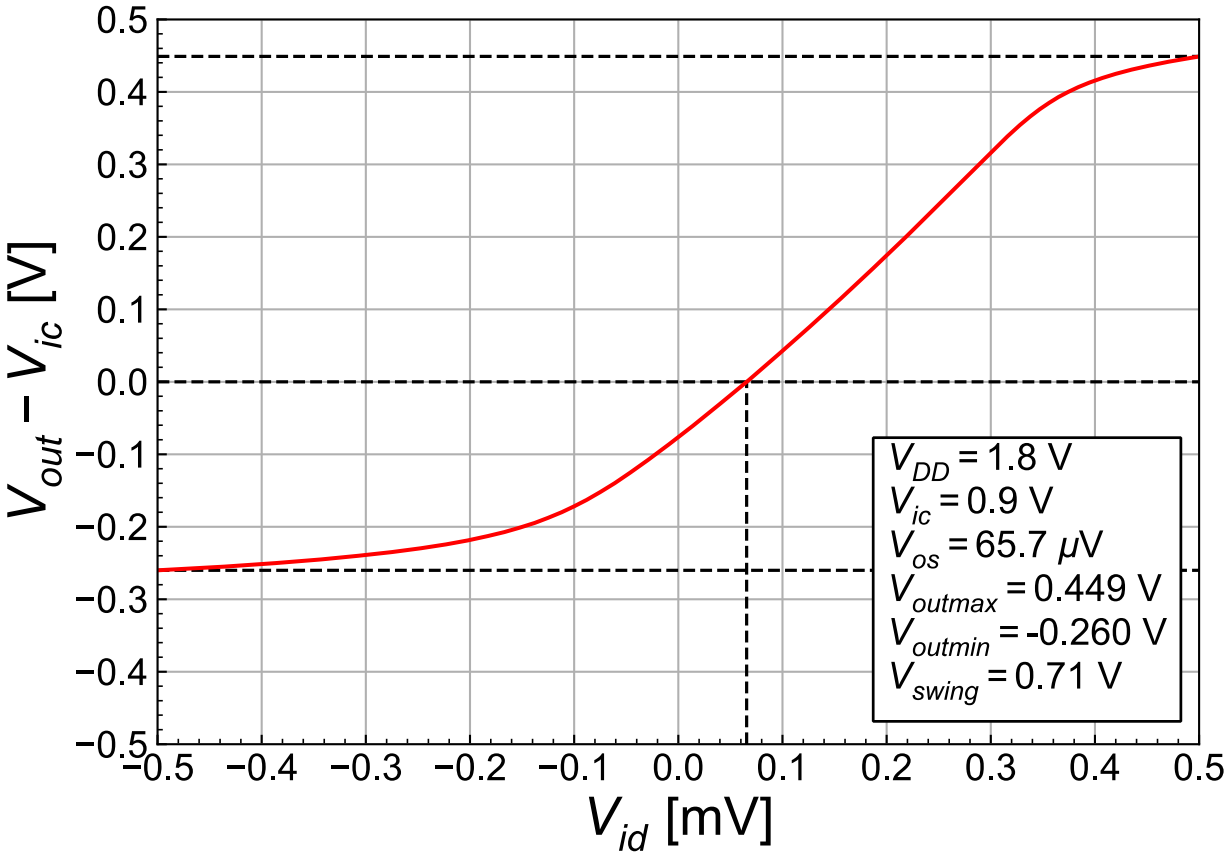
Transistor sizes

	Type	Function	W	L	ID	W/L	Ispec	IC	VP-VS	VG-VT0	VDSsat	Gspec	Gms	Gm	Gds	gamman
M1a	n	DP	10.5E-6	3.0E-6	250.0E-9	3.50	2.503E-6	0.10	-57.1E-3	-44.9E-3	104.8E-3	96.7E-6	8.9E-6	7.0E-6	3.47E-9	0.65
M1b	n	DP	10.5E-6	3.0E-6	250.0E-9	3.50	2.503E-6	0.10	-57.1E-3	-44.9E-3	104.8E-3	96.7E-6	8.9E-6	7.0E-6	3.47E-9	0.65
M2a	p	CM	200.0E-9	7.6E-6	250.0E-9	0.03	4.556E-9	54.87	408.4E-3	312.7E-3	397.1E-3	176.1E-9	1.2E-6	933.6E-9	1.64E-9	0.84
M2b	p	CM	200.0E-9	7.6E-6	250.0E-9	0.03	4.556E-9	54.87	408.4E-3	312.7E-3	397.1E-3	176.1E-9	1.2E-6	933.6E-9	1.64E-9	0.84
M3a	n	CM	200.0E-9	17.5E-6	500.0E-9	0.01	8.171E-9	61.19	431.3E-3	339.3E-3	417.8E-3	315.8E-9	2.3E-6	1.8E-6	1.19E-9	0.82
M3b	n	CM	200.0E-9	17.5E-6	500.0E-9	0.01	8.171E-9	61.19	431.3E-3	339.3E-3	417.8E-3	315.8E-9	2.3E-6	1.8E-6	1.19E-9	0.82

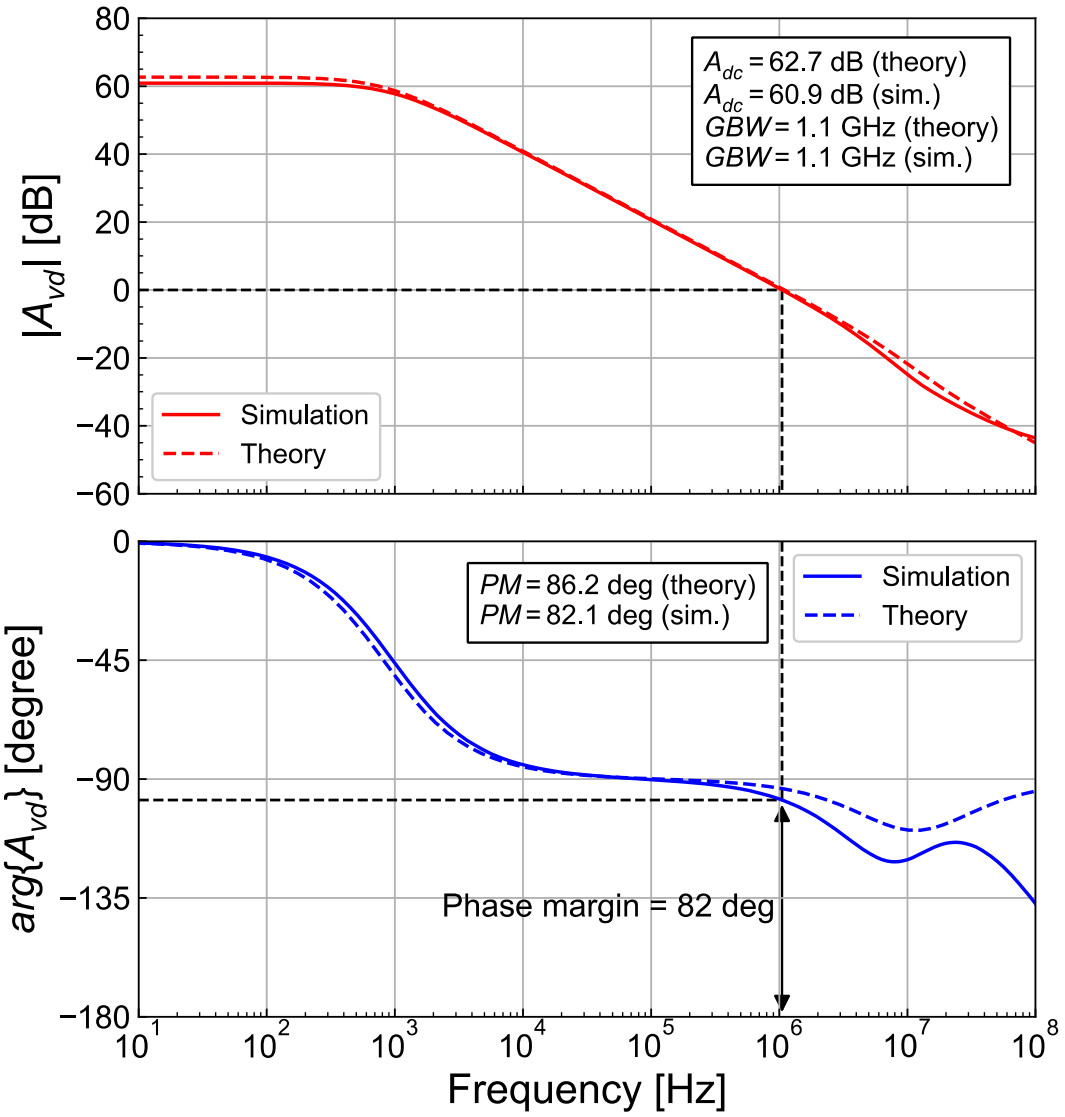
Simulations – Large-signal Transfer Characteristic



Simulations – Large-signal Transfer Characteristic (zoom)



Simulations – OL SS Transfer Function



Input-referred Thermal Noise

- To evaluate the thermal noise, we first compute $G_{m1} = 6.96\ \mu A/V$, $G_{m2} = 933\ nA/V$, $\gamma_{n1} = 0.65$, $\gamma_{n2} = 0.84$ from which we get $\eta_{th} = 0.173$, which means that the contribution of the current mirror remains small
- The OTA thermal noise excess noise factor is then given by

$$\gamma_{ota} = 2\gamma_{n1}(1 + \eta_{th}) = 1.53$$

- which is only slightly larger than the contribution of the differential pair
- The input thermal noise resistance is

$$R_{nt} = \frac{\gamma_{ota}}{G_{m1}} = 220\ k\Omega$$

- which corresponds to $\sqrt{S_{nt}} = \sqrt{4kTR_{nt}} = 60.4\ \frac{nV}{\sqrt{Hz}}$
- In the Smash simulator we have plotted $10\log(S_{nt}) = -144.4\ \frac{dBv}{\sqrt{Hz}}$

Input-referred Flicker Noise

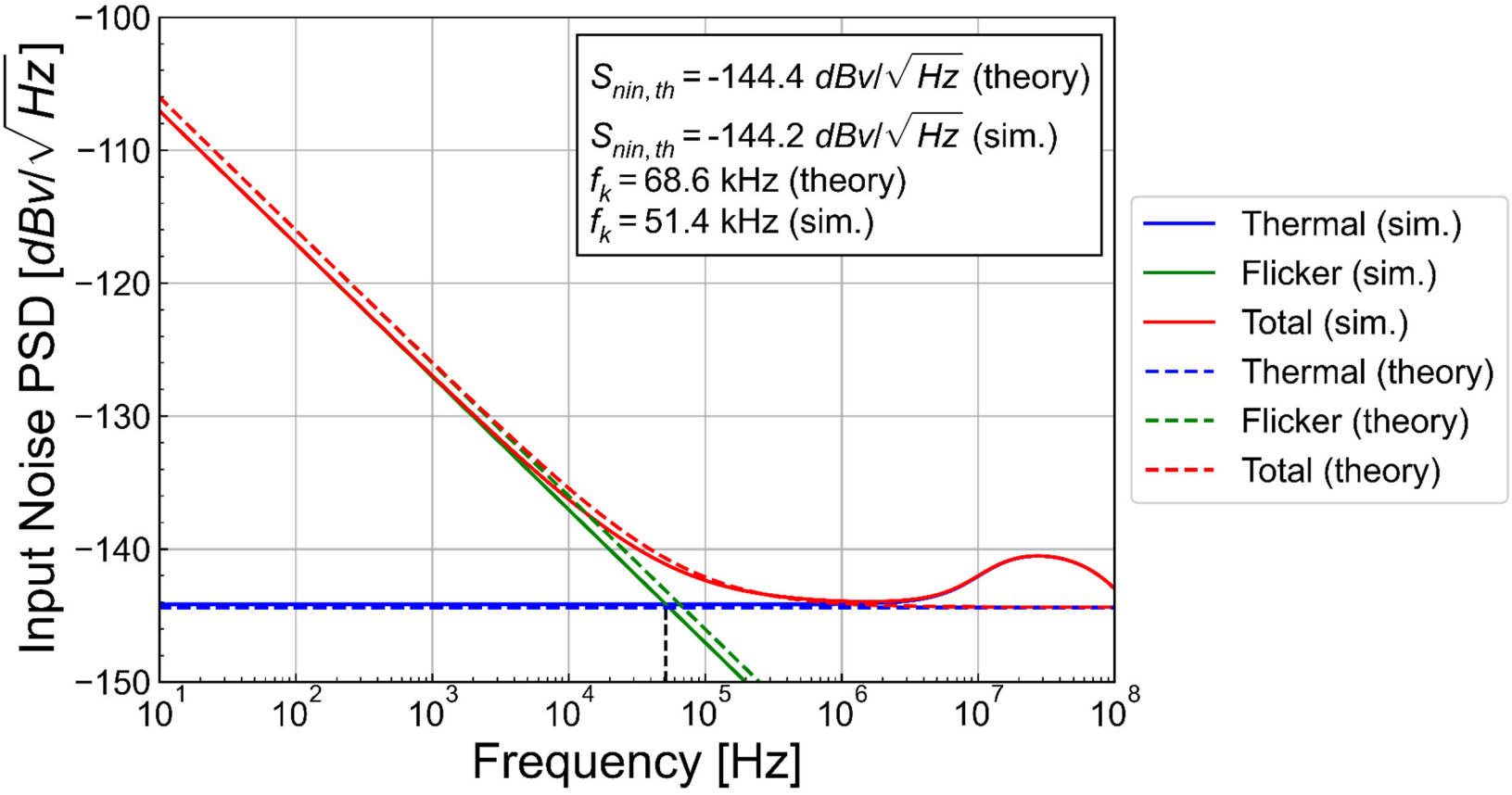
- The contribution to the input-referred flicker noise of the current mirror relative to the differential pair is obtained as

$$\eta_{fl} = \left(\frac{G_{m2}}{G_{m1}}\right)^2 \frac{\rho_p}{\rho_n} \frac{W_1 L_1}{W_2 L_2} = 3.1$$

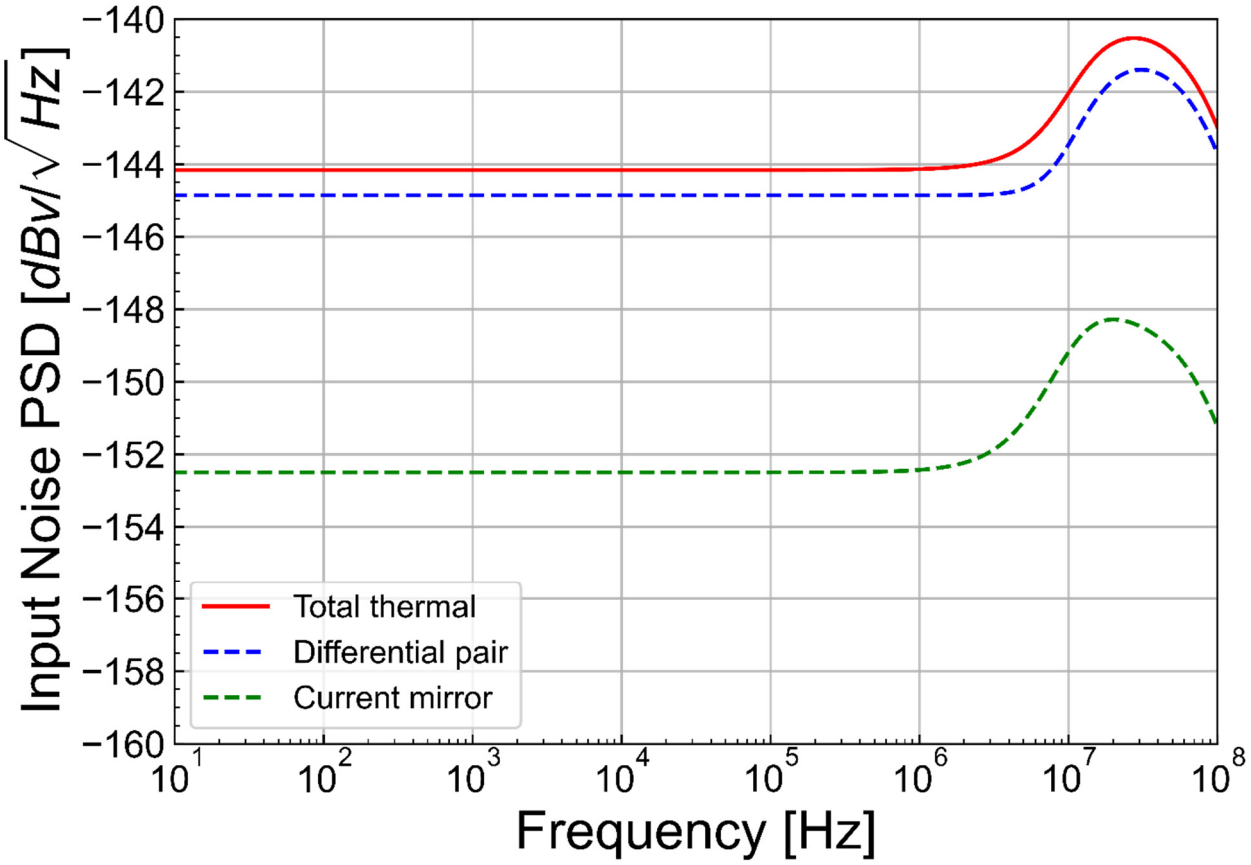
- which means that the current mirror contributes 3 times more than the differential pair
- This is partly due to the fact that for this technology the pMOS flicker noise is 8.3 times larger than the nMOS (ρ_p about 8.3 times larger than ρ_n)
- The resulting corner frequency is then given by

$$f_k = \frac{2\rho_n}{W_1 L_1 R_{nt}} \cdot (1 + \eta_{fl}) = \frac{G_{m1}}{\gamma_{ota}} \frac{2\rho_n}{W_1 L_1} \cdot (1 + \eta_{fl}) = 68.6\ kHz$$

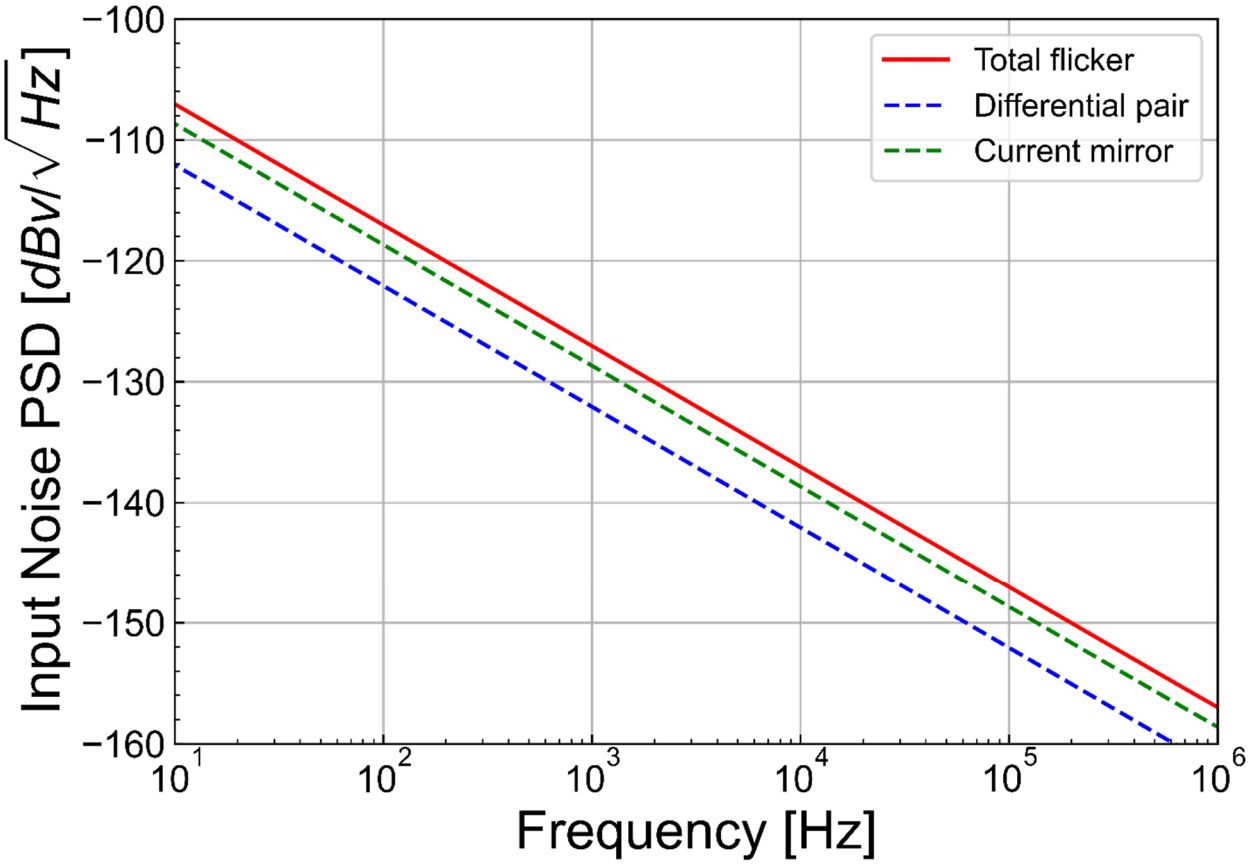
Simulations – Input-referred Noise



Simulations – Input-referred Thermal Noise



Simulations – Input-referred Flicker Noise



Input-referred Offset Voltage

- To evaluate the input referred offset voltage we first calculate

$$\sigma_{\beta_1} = \frac{A_{\beta n}}{\sqrt{W_1 L_1}} = 1.782 \times 10^{-3} \text{ and } \sigma_{V_{T1}} = \frac{A_{V_{Tn}}}{\sqrt{W_1 L_1}} = 0.891\, mV$$

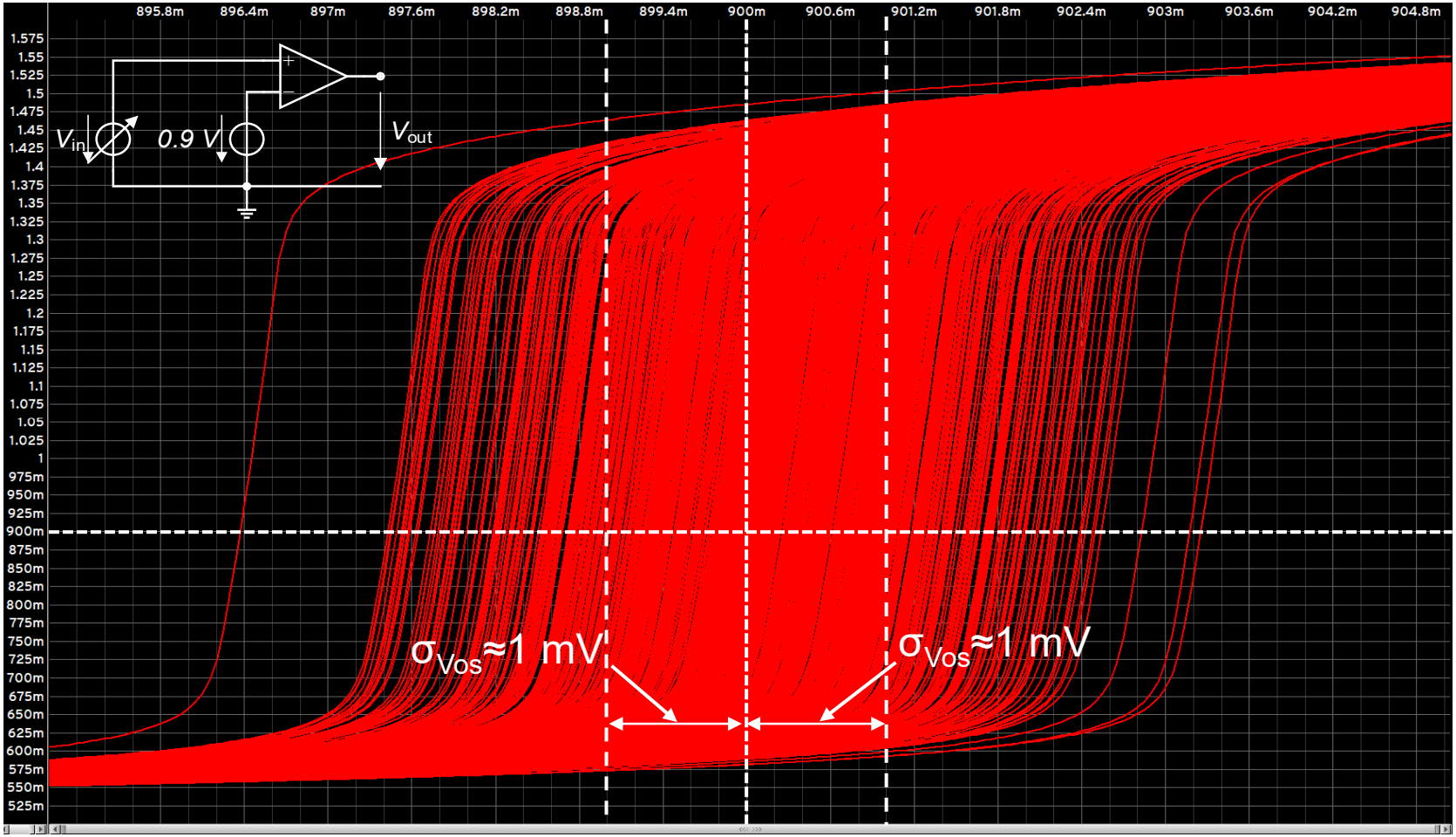
$$\sigma_{\beta_2} = \frac{A_{\beta p}}{\sqrt{W_2 L_2}} = 8.111 \times 10^{-3} \text{ and } \sigma_{V_{T2}} = \frac{A_{V_{Tp}}}{\sqrt{W_2 L_2}} = 4.056\, mV$$

- The input-referred offset voltage is then given by

$$\sigma_{V_{os}} = \sqrt{\left(\frac{I_b}{G_{m1}}\right)^2 \left(\sigma_{\beta_1}^2 + \sigma_{\beta_2}^2\right) + \left(\frac{G_{m2}}{G_{m1}}\right)^2 \sigma_{V_{T2}}^2 + \sigma_{V_{T1}}^2} = 1.085\, mV$$

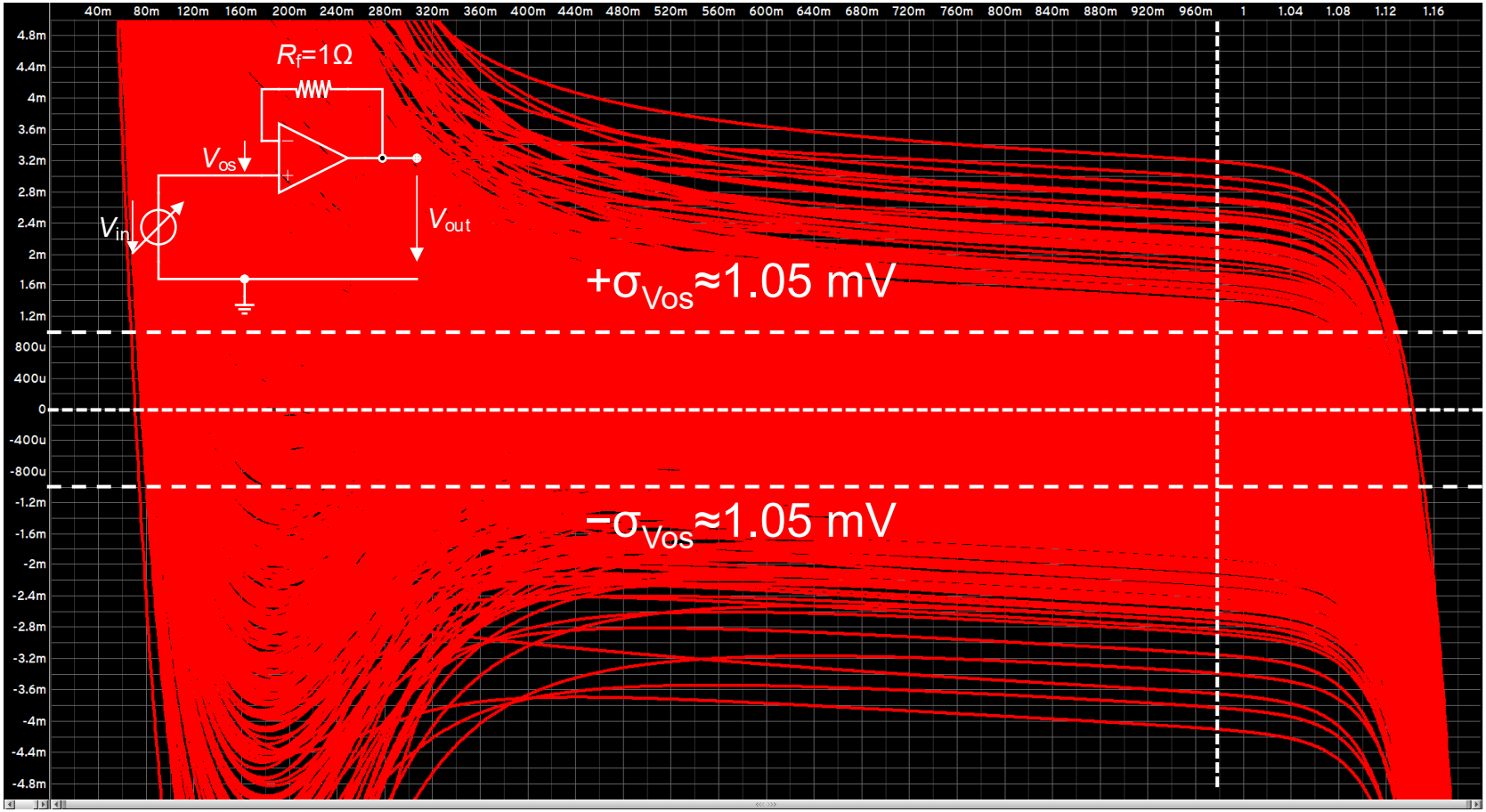
- which as expected is dominated by the offset voltage of the differential pair and which is below the target specification

Simulations – MC Simulation of Offset Voltage (open-loop)



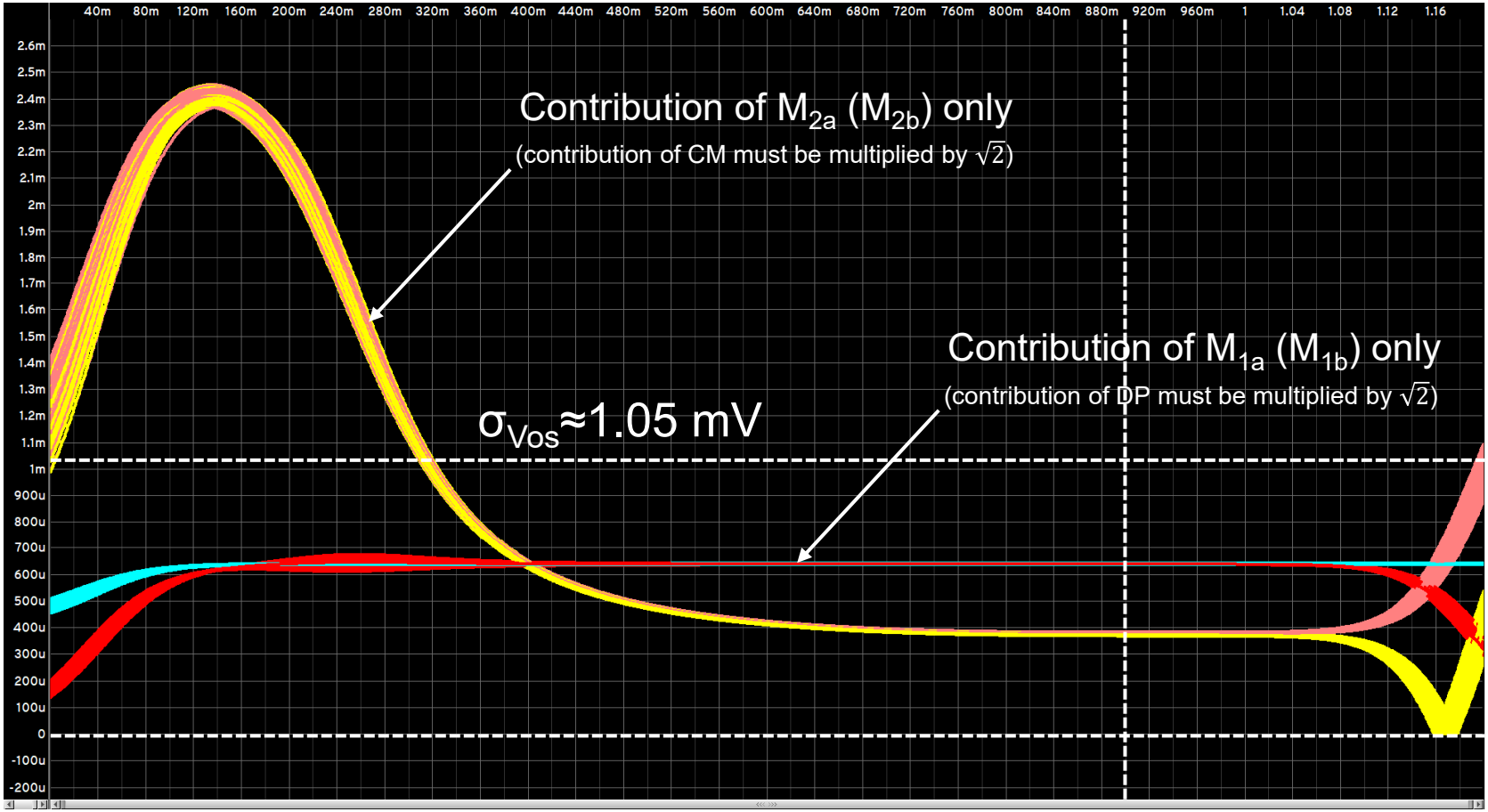
- Offset simulation using Monte Carlo simulations with 1000 runs
- The standard deviation is of V_{os} is about 1.07 mV, which is consistent with the dispersion simulation giving 1.05 mV and close to the 1.08 mV theoretical prediction

Monte Carlo Simulation of Offset Voltage (closed-loop)



- Monte Carlo simulation of V_{os} versus V_{in} for 1000 runs in voltage follower mode
- The standard deviation of V_{os} is about 1.07 mV, which is consistent with the dispersion simulation giving 1.05 mV and close to the 1.08 mV theoretical prediction

Monte Carlo Simulation of Offset Voltage



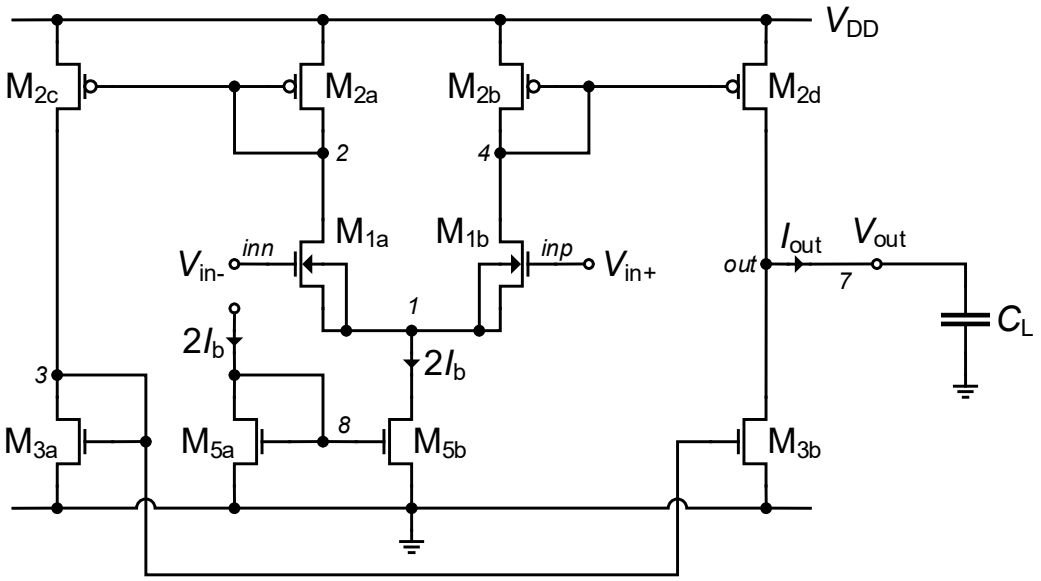
- Offset simulation using Monte Carlo simulations with 1000 runs
- As expected the contribution of the differential pair (M_{1a}-M_{1b}) dominates within the linear range

Outline

- Introduction
- Settling time of OTA with capacitive feedback
- The single-stage or simple OTA
- **The symmetrical OTA**

The Symmetrical Differential OTA

Current mirrors current gains defined as:
$A_1=\beta_{2c}/\beta_{2a}$
$A_2=\beta_{3b}/\beta_{3a}$
$A_3=\beta_{2d}/\beta_{2b}$
with
$A_3=A_1 \cdot A_2$



- The symmetrical OTA offers a higher output voltage swing
- Its transconductance can be boosted thanks to the current mirrors current gains which can be set to values larger than one

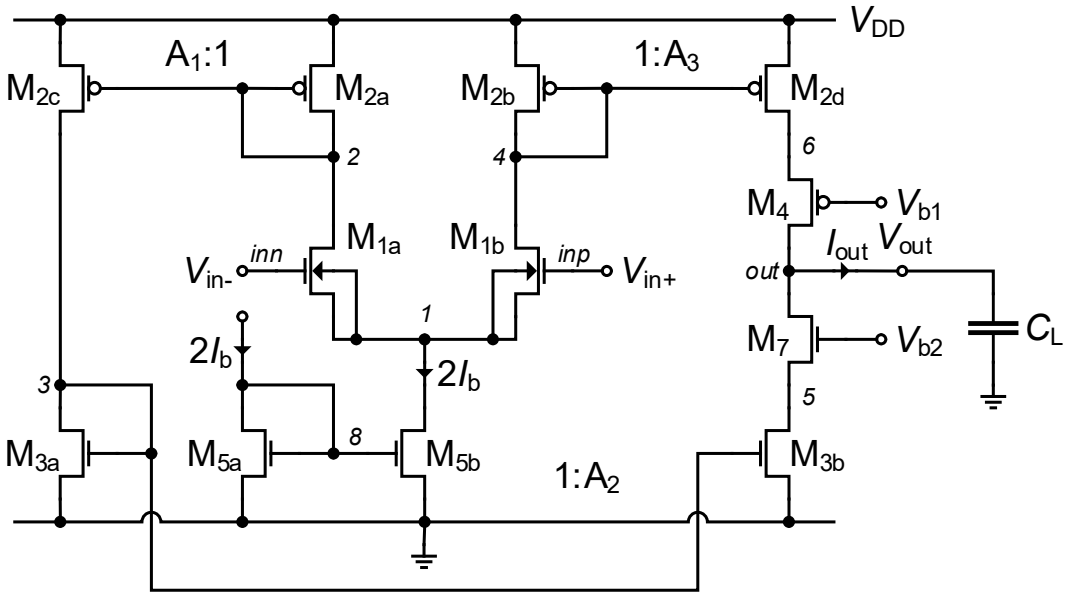
$$G_m \triangleq \frac{I_{out}}{V_{id}} = A_3 \cdot G_{m1}$$

- This is achieved at the cost of a larger noise

F. Krummenacher, "High voltage gain CMOS OTA for micropower SC filters," Electronics Letters, Vol. 17, pp. 160-162, 1981.

The Symmetrical Differential Cascode OTA

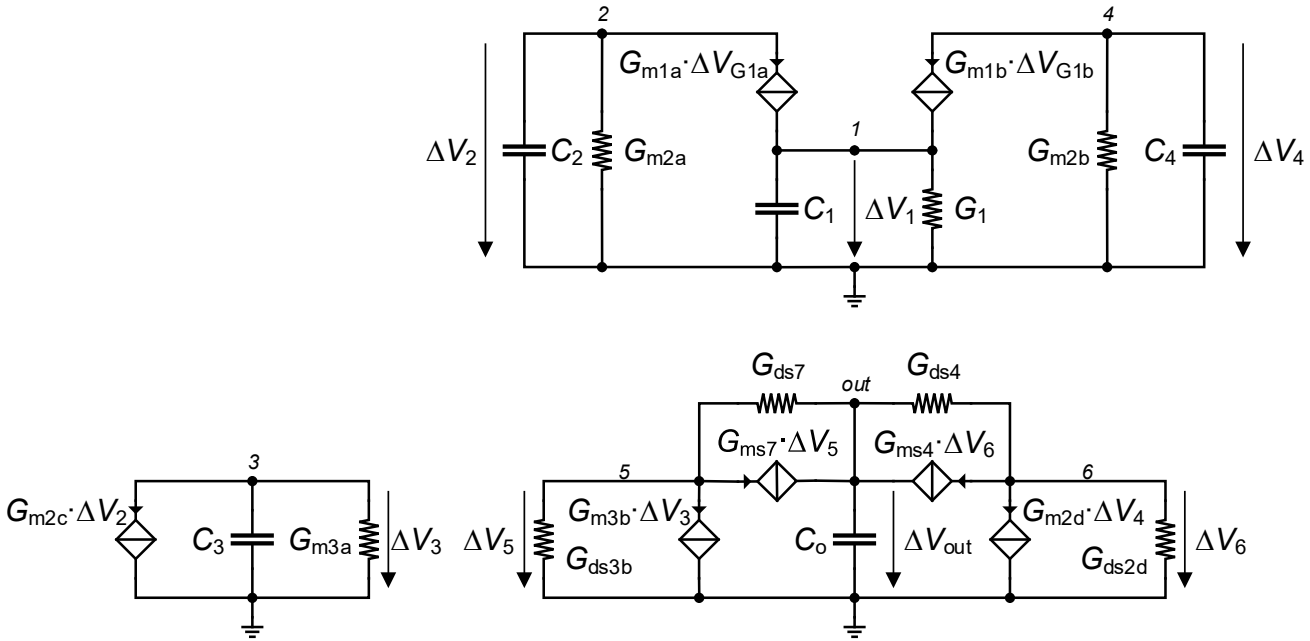
Current mirrors current gains defined as:
$A_1=\beta_{2c}/\beta_{2a}$
$A_2=\beta_{3b}/\beta_{3a}$
$A_3=\beta_{2d}/\beta_{2b}$
with
$A_3=A_1\cdot A_2$



- Cascode transistors M_4 and M_7 are added to increase the output resistance and hence improve the dc gain at the cost of a reduced output swing
- In the following analysis, we will assume that $M_{1a}\equiv M_{1b}$ and $M_{2a}\equiv M_{2b}$ and hence $G_{m1a}=G_{m1b}=G_{m1}, W_{1a}=W_{1b}=W_1, L_{1a}=L_{1b}=L_1, G_{m2a}=G_{m2b}=G_{m2}, W_{2a}=W_{2b}=W_2, L_{2a}=L_{2b}=L_2$
- Additionally we will use $G_{m3}=G_{m3a}$

F. Krummenacher, “High voltage gain CMOS OTA for micropower SC filters,” Electronics Letters, Vol. 17, pp. 160-162, 1981.

Small-signal Equivalent Schematic



$$G_{m1b} = G_{m1a} = G_{m1} \gg G_1$$
$$G_{m2b} = G_{m2a} = G_{m2}$$
$$G_{m2d} = A_3 G_{m2b} = A_3 G_{m2}$$
$$G_{m2c} = A_1 G_{m2a} = A_1 G_{m2}$$
$$G_{m3b} = A_2 G_{m3a} = A_2 G_{m3}$$
$$A_3 = A_1 A_2$$
$$G_{mi} \gg G_{dsi} \text{ for } i = 1..10$$

Small-signal Transfer Function

- The small-signal output voltage can be evaluated from the above small-signal equivalent circuit

$$\Delta V_{out} = \frac{A_{dc}}{1+s\tau_o}\left[\frac{\Delta V_{in+}}{1+s\tau_{p4}} - \frac{\Delta V_{in-}}{(1+s\tau_{p2})(1+s\tau_{p3})} - \frac{\Delta V_{in+}+\Delta V_{in-}}{2(1+s\tau_{p1})}\left(\frac{1}{1+s\tau_{p4}} - \frac{1}{(1+s\tau_{p2})(1+s\tau_{p3})}\right)\right]$$

- where $A_{dc} = G_m/G_o$
- is the dc gain and $G_m = A_3 G_{m1}$
- the OTA equivalent transconductance and

$$G_o = \frac{G_{ds3b}G_{ds7}}{G_{ms7}} + \frac{G_{ds2d}G_{ds4}}{G_{ms4}}$$

- the total output conductance and $\tau_o = C_o/G_o$ the time constant corresponding to the dominant pole ω_0
- The other time constants are given by

$$\tau_{p1} = C_1/(2G_{m1}),\ \tau_{p2} = C_2/G_{m2},\ \tau_{p3} = C_3/G_{m3},\ \tau_{p4} = C_4/G_{m2}$$

- In most practical cases, we usually have $\tau_o \gg \tau_{p2}, \tau_{p3}, \tau_{p4} > \tau_{p1}$

Transfer Function Approximation

- The small-signal output voltage can be written as

$$\Delta V_{out} = \frac{A_0}{1 + s\tau_o}\left[F(s) \cdot \Delta V_{in+} - G(s) \cdot \Delta V_{in-}\right]$$

- where $F(s) = \frac{1}{1+s\tau_{p4}} - \frac{1}{2}\frac{1}{1+s\tau_{p1}}\left(\frac{1}{1+s\tau_{p4}} - \frac{1}{(1+s\tau_{p2})(1+s\tau_{p3})}\right)$

$$G(s) = \frac{1}{(1 + s\tau_{p2})(1 + s\tau_{p3})} + \frac{1}{2}\frac{1}{1 + s\tau_{p1}}\left(\frac{1}{1 + s\tau_{p4}} - \frac{1}{(1 + s\tau_{p2})(1 + s\tau_{p3})}\right)$$

- The above transfer functions can be simplified according to

$$\prod_{k=1}^{n}(1 + s\tau_{pk}) \cong 1 + s\sum_{k=1}^{n}\tau_{pk} \text{ for } \omega \leq \frac{1}{2\sum_{k=1}^{n}\tau_{pk}}$$

- which leads to

$$F(s) \cong G(s) \cong \frac{1 + s\tau_n}{1 + s\tau_d}$$

- where $\tau_n = \tau_{p1} + \frac{\tau_{p2}+\tau_{p3}+\tau_{p4}}{2}$ and $\tau_d = \tau_{p1} + \tau_{p2} + \tau_{p3} + \tau_{p4}$

Transfer Function Approximation

- For $\omega \leq \frac{1}{2\tau_d}$, the above expression can be further simplified considering that

$$\frac{1+s\tau_n}{1+s\tau_d} \cong \frac{1}{1+s(\tau_d-\tau_n)}$$

- where

$$\tau_d - \tau_n = \frac{\tau_{p2}+\tau_{p3}+\tau_{p4}}{2} = \frac{\tau_p}{2}$$

- τ_p represents the sum of the time constants associated with all the current mirrors
- $F(s)$ and $G(s)$ then writes

$$F(s) \cong G(s) \cong \frac{1}{1+s\frac{\tau_p}{2}}$$

- which is valid for $\omega \leq \frac{1}{2\tau_d} = \frac{1}{2(\tau_{p1}+\tau_p)}$

Approximate Differential Transfer Function

- The simplified transfer function is then given by

$$A_{dm}(s) \triangleq \frac{\Delta V_{out}}{\Delta V_{id}} \cong \frac{A_{dc}}{(1+s\tau_o)\left(1+s\frac{\tau_p}{2}\right)} = \frac{A_{dc}}{\left(1+\frac{s}{\omega_0}\right)\left(1+\frac{s}{\omega_p}\right)}$$

- with $\omega_0 = 1/\tau_0$ and $\omega_p = 2/\tau_p$
- where it is assumed that $\tau_p = \tau_{p2} + \tau_{p3} + \tau_{p4} \ll \tau_o$
- $\omega_0 = 1/\tau_o \ll \omega_p$ is the **dominant pole** which is set by the load capacitance at the OTA output whereas $\omega_p = 2/\tau_p$ represents the **non-dominant pole** due to all the time constants due to the parasitic capacitances at the current mirror nodes
- The transfer function can be further simplified as

$$A_{dm}(s) \cong \frac{1}{s\tau_u\left(1+s\frac{\tau_p}{2}\right)} = \frac{1}{\frac{s}{\omega_u}\left(1+\frac{s}{\omega_p}\right)}$$

- where $\omega_u = 1/\tau_u = A_{dc}\omega_0 = G_m/C_o$ is the **unity-gain frequency** or gain-bandwidth product which is set by the OTA transconductance G_m and the toal load capacitance C_o

Noise Analysis

- Neglecting the contribution of the cascode transistors M_4 and M_7, the PSD of the output noise current is given by

$$S_{I_{nout}} = A_3^2\left(S_{I_{n1a}} + S_{I_{n1b}} + S_{I_{n2a}} + S_{I_{n2b}}\right) + A_2^2\left(S_{I_{n2c}} + S_{I_{n3a}}\right) + S_{I_{n2d}} + S_{I_{n3b}}$$

- or if we express the output PSD in terms of the output noise conductance

$$S_{I_{nout}} = 4kT \cdot G_{nout}$$

- where

$$G_{nout} = 2A_3^2 \cdot (G_{n1} + G_{n2}) + A_2^2 \cdot (G_{n2c} + G_{n3a}) + G_{n2d} + G_{n3b}$$

- where we have assumed that $M_{1a} \equiv M_{1b}$ $M_{2a} \equiv M_{2b}$ and with

$$G_{ni} = \gamma_{ni} G_{mi} + G_{mi}^2 \frac{\rho_i}{W_i L_i f}$$ for all transistors

- The input-referred noise is then given by

$$R_{nin} \triangleq \frac{G_{nout}}{A_3^2 \cdot G_{m1}^2} = \frac{2(G_{n1} + G_{n2})}{G_{m1}^2} + \frac{G_{n2c} + G_{n3a}}{A_1^2 \cdot G_{m1}^2} + \frac{G_{n2d} + G_{n3b}}{A_3^2 \cdot G_{m1}^2}$$

- where we have used $A_3 = A_1 \cdot A_2$

Input-referred Thermal Noise

- The input-referred thermal noise resistance is given by

$$R_{nth} = \frac{2\gamma_{n1}}{G_{m1}} \cdot (1 + \eta_{th})$$

- where

$$\eta_{th} = \frac{\gamma_{n2}}{\gamma_{n1}}\frac{G_{m2}}{G_{m1}} + \frac{1}{2A_1^2}\left(\frac{\gamma_{n2c}}{\gamma_{n1}}\frac{G_{m2c}}{G_{m1}} + \frac{\gamma_{n3a}}{\gamma_{n1}}\frac{G_{m3a}}{G_{m1}}\right) + \frac{1}{2A_3^2}\left(\frac{\gamma_{n2d}}{\gamma_{n1}}\frac{G_{m2d}}{G_{m1}} + \frac{\gamma_{n3b}}{\gamma_{n1}}\frac{G_{m3b}}{G_{m1}}\right)$$

- represents the contributions to the input-referred thermal noise of the current mirrors relative to that of the differential pair
- Now $G_{m2c} = A_1 \cdot G_{m2a} = A_1 \cdot G_{m2}$, $G_{m3b} = A_2 \cdot G_{m3a} = A_2 \cdot G_{m3}$ and $G_{m2d} = A_3 \cdot G_{m2b} = A_3 \cdot G_{m2}$ and assuming that $\gamma_{n2a} = \gamma_{n2b} \cong \gamma_{n2c} \cong \gamma_{n2d} = \gamma_{n2}$ and $\gamma_{n3a} \cong \gamma_{n3b} = \gamma_{n3}$ then η_{th} reduces to

$$\eta_{th} \cong \frac{\gamma_{n2}}{2\gamma_{n1}}\frac{G_{m2}}{G_{m1}} \cdot \left(2 + \frac{1}{A_1} + \frac{1}{A_3}\right) + \frac{1}{2A_1^2}\frac{\gamma_{n3}}{\gamma_{n1}}\frac{G_{m3}}{G_{m1}} \cdot \left(1 + \frac{1}{A_2}\right)$$

Input-referred Thermal Noise ($A_1 = A_2 = A_3 = 1$)

- In case $A_1 = A_2 = A_3 = 1$ then η_{th} reduces to

$$\eta_{th} = 2\frac{\gamma_{n2}}{\gamma_{n1}}\frac{G_{m2}}{G_{m1}} + \frac{\gamma_{n3}}{\gamma_{n1}}\frac{G_{m3}}{G_{m1}}$$

- In case $G_{m1} \gg G_{m2}$ and $G_{m1} \gg G_{m3}$, the thermal noise is dominated by the input differential pair and the previous expression can be simplified

$$R_{nth} \cong \frac{2\gamma_{n1}}{G_{m1}}$$

Thermal Noise Excess Factor

- To compare with other OTA it is useful to derive the thermal noise excess factor

$$\gamma_{ota} \triangleq G_m \cdot R_{nth}$$

- where $G_m = A_3 \cdot G_{m1}$ is the OTA transconductance
- This results in

$$\gamma_{ota} = 2A_3 \cdot \gamma_{n1} \cdot (1 + \eta_{th})$$

- In case $G_{m1} \gg G_{m2}$ and $G_{m1} \gg G_{m3}$, the noise is dominated by the input differential pair and the previous expression can be simplified

$$\gamma_{ota} \cong 2A_3 \cdot \gamma_{n1}$$

- We see that γ_{ota} is proportional to the current gain A_3
- Introducing current gains improves the transconductance at the cost of higher noise

Input-referred Flicker Noise

- The input-referred flicker noise is given by

$$f \cdot R_{nfl} = \frac{2\rho_n}{W_1 L_1} + \rho_p \left(\frac{G_{m2}}{G_{m1}}\right)^2 \left(\frac{2}{W_2 L_2} + \frac{1}{W_{2c} L_{2c}} + \frac{1}{W_{2d} L_{2d}}\right) + \frac{\rho_n}{A_1^2} \left(\frac{G_{m3}}{G_{m1}}\right)^2 \left(\frac{1}{W_{3a} L_{3a}} + \frac{1}{W_{3b} L_{3b}}\right)$$

- which can be written as

$$R_{nfl} = \frac{2\rho_n}{W_1 L_1 f} \cdot (1 + \eta_{fl})$$

- where

$$\eta_{fl} = \frac{\rho_p}{2\rho_n} \left(\frac{G_{m2}}{G_{m1}}\right)^2 \left(\frac{2W_1 L_1}{W_2 L_2} + \frac{W_1 L_1}{W_{2c} L_{2c}} + \frac{W_1 L_1}{W_{2d} L_{2d}}\right) + \frac{1}{2A_1^2} \left(\frac{G_{m3}}{G_{m1}}\right)^2 \left(\frac{W_1 L_1}{W_{3a} L_{3a}} + \frac{W_1 L_1}{W_{3b} L_{3b}}\right)$$

- represents the contributions to the input-referred flicker noise of the current mirrors relative to that of the differential pair
- For $A_1 = A_2 = A_3 = 1$, $M_{2a} \equiv M_{2b} \equiv M_{2c} \equiv M_{2d}$ and $M_{3a} \equiv M_{3b}$, $W_{2a} = W_{2b} = W_{2c} = W_{2d} = W_2$, $L_{2a} = L_{2b} = L_{2c} = L_{2d} = L_2$, $W_{3a} = W_{3b} = W_3$, $L_{3a} = L_{3b} = L_3$ then η_{fl} reduces to

$$\eta_{fl} = 2\frac{\rho_p}{\rho_n} \left(\frac{G_{m2}}{G_{m1}}\right)^2 \frac{W_1 L_1}{W_2 L_2} + \left(\frac{G_{m3}}{G_{m1}}\right)^2 \frac{W_1 L_1}{W_3 L_3}$$

Input-referred Offset Voltage

- The input-referred voltage can be obtained in a similar way than noise
- The variance of the input-referred offset voltage is given by

$$\sigma_{V_{os}}^2 = \sigma_{V_{T1}}^2 \cdot \left(1 + \xi_{V_T}\right) + \left(\frac{I_b}{G_{m1}}\right)^2 \cdot \sigma_{\beta_1}^2 \cdot \left(1 + \xi_\beta\right)$$

- where ξ_{V_T} represents the V_T mismatch contributions to the input-referred offset of the current mirror relative to that of the differential pair

$$\xi_{V_T} = 2\left(\frac{G_{m2}}{G_{m1}}\right)^2 \cdot \frac{\sigma_{V_{T2}}^2}{\sigma_{V_{T1}}^2} + \left(\frac{G_{m3}}{A_1\, G_{m1}}\right)^2 \cdot \frac{\sigma_{V_{T3}}^2}{\sigma_{V_{T1}}^2}$$

- and ξ_β represents the β mismatch contributions to the input-referred offset of the current mirror relative to that of the differential pair

$$\xi_\beta = 2\frac{\sigma_{\beta_2}^2}{\sigma_{\beta_1}^2} + \frac{\sigma_{\beta_3}^2}{A_1^2\, \sigma_{\beta_1}^2}$$

Input-referred Offset Voltage

- with

$$\sigma_{V_{T1}}^2 = \frac{A_{V_{Tn}}^2}{W_1 L_1} \quad \sigma_{V_{T2}}^2 = \frac{A_{V_{Tp}}^2}{W_2 L_2} \quad \sigma_{V_{T3}}^2 = \frac{A_{V_{Tn}}^2}{W_3 L_3}$$

$$\sigma_{\beta_1}^2 = \frac{A_{\beta_n}^2}{W_1 L_1} \quad \sigma_{\beta_2}^2 = \frac{A_{\beta_p}^2}{W_2 L_2} \quad \sigma_{\beta_3}^2 = \frac{A_{\beta_n}^2}{W_3 L_3}$$

- Replacing results in

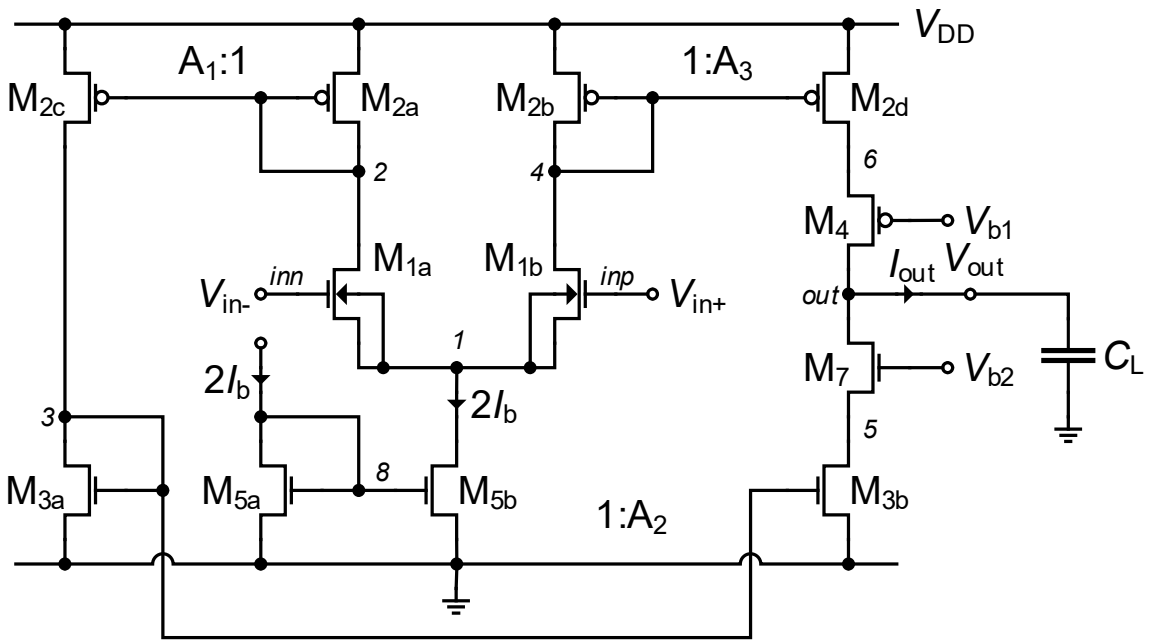
$$\xi_{V_T} = 2\left(\frac{G_{m2}}{G_{m1}}\right)^2 \cdot \left(\frac{A_{V_{Tp}}}{A_{V_{Tn}}}\right)^2 \cdot \frac{W_1 L_1}{W_2 L_2} + \left(\frac{G_{m3}}{A_1\, G_{m1}}\right)^2 \cdot \frac{W_1 L_1}{W_3 L_3}$$

- and

$$\xi_\beta = 2\left(\frac{A_{\beta_p}}{A_{\beta_n}}\right)^2 \cdot \frac{W_1 L_1}{W_2 L_2} + \frac{1}{A_1^2} \cdot \frac{W_1 L_1}{W_3 L_3}$$

- Similarly to the flicker noise, the input-referred offset (variance or standard deviation) can be reduced by increasing the M_{1a}-M_{1b} area $W_1 L_1$ but at the same time also increasing the area of the current mirrors $W_2 L_2$ (and hence $W_{2c} L_{2c}$ and $W_{2d} L_{2d}$) and depending on A_1 also the area of M_{3a}-M_{3b} $W_{3a} L_{3a}$ and $W_{3b} L_{3b}$

Design Example

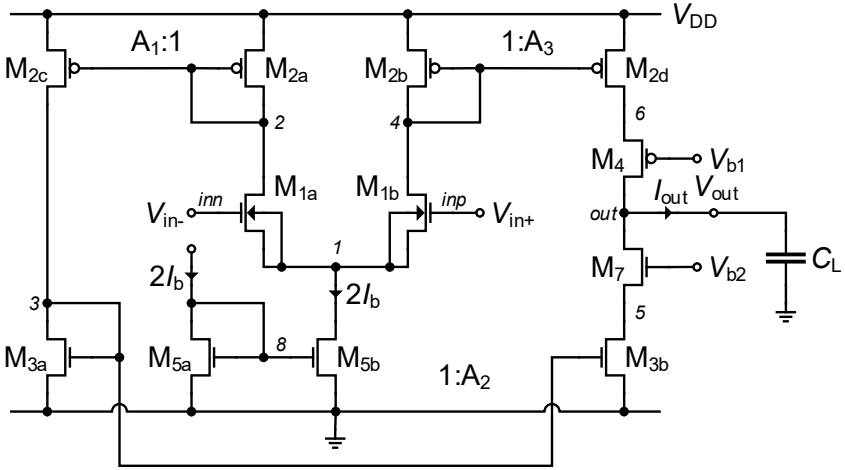


- Design the above symmetrical OTA for unity gain current mirrors $A_1 = A_2 = A_3 = 1$ with the following specifications

$$A_{dc} \geq 100\,dB, GBW \geq 1\,MHz, V_{os} \leq 10\,mV$$

- for a load capacitance $C_L = 1\,pF$ and for the process parameters corresponding to a 180nm CMOS process
- The design procedure is detailed in the Jupyter Notebook

Sizing Summary



$$A_1 = A_2 = A_3 = 1$$

Specifications

Name	Value
AdcdB	100
GBWmin	1.00E+06
CL	1E-12
VDD	1.8
Wmin	2E-07
Lmin	1.8E-07
Vosmax	0.01
PMdeg	60

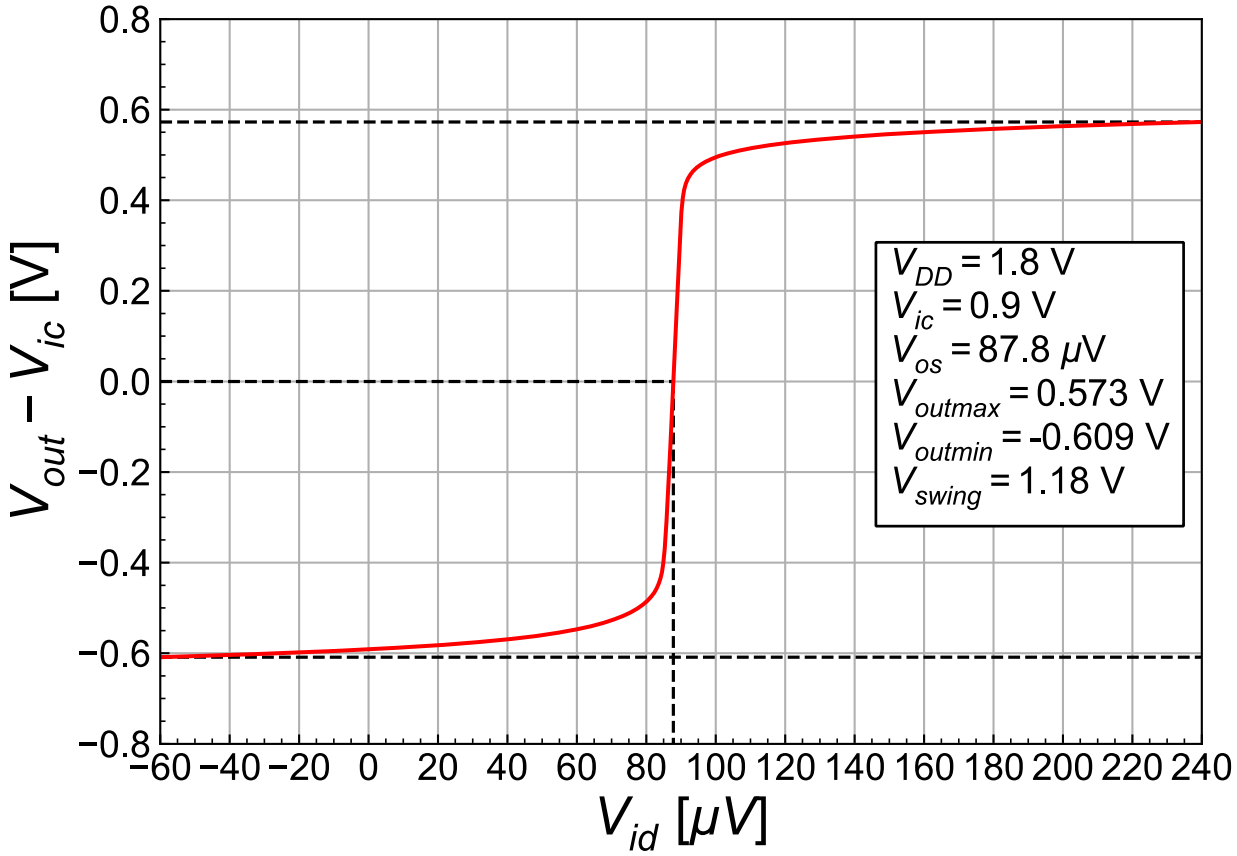
Bias

Name	Value
VDD	1.8
VSS	0
Ib	2.5E-07
Vb1	0.9
Vb2	0.9

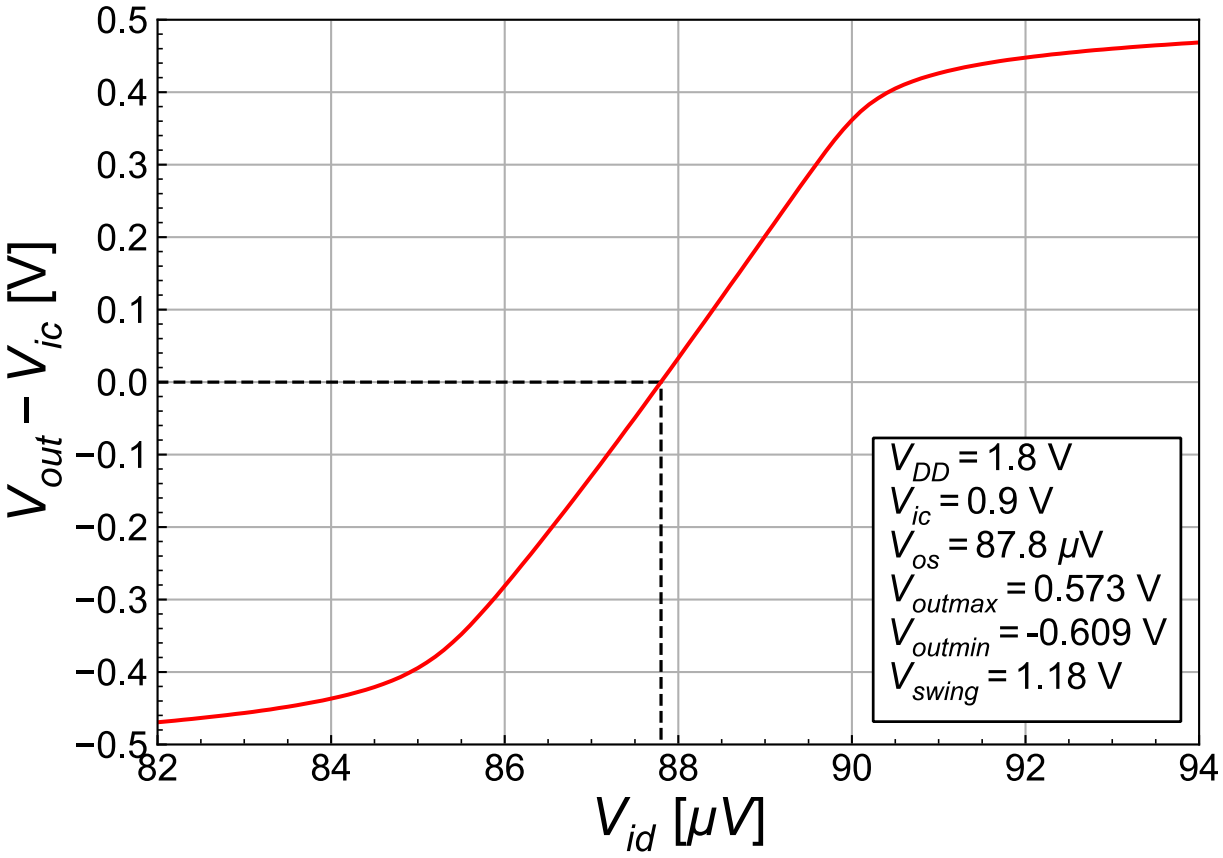
Transistor sizes

	Type	Function	W	L	ID	W/L	Ispec	IC	VP-VS	VG-VT0	VDSsat	Gspec	Gms	Gm	Gds	gamman
M1a	n	DP	2.78E-06	8.00E-07	2.50E-07	3.48	2.48E-06	0.10	-0.057	-0.045	0.105	9.60E-05	8.85E-06	6.96E-06	2.60E-08	0.65
M1b	n	DP	2.78E-06	8.00E-07	2.50E-07	3.48	2.48E-06	0.10	-0.057	-0.045	0.105	9.60E-05	8.85E-06	6.96E-06	2.60E-08	0.65
M2a	p	CM	3.10E-07	5.00E-06	2.50E-07	0.06	1.07E-08	23.29	0.263	0.202	0.270	4.15E-07	1.81E-06	1.38E-06	5.00E-09	0.83
M2b	p	CM	3.10E-07	5.00E-06	2.50E-07	0.06	1.07E-08	23.29	0.263	0.202	0.270	4.15E-07	1.81E-06	1.38E-06	5.00E-09	0.83
M2c	p	CM	3.10E-07	5.00E-06	2.50E-07	0.06	1.07E-08	23.29	0.263	0.202	0.270	4.15E-07	1.81E-06	1.38E-06	5.00E-09	0.83
M2d	p	CM	3.10E-07	5.00E-06	2.50E-07	0.06	1.07E-08	23.29	0.263	0.202	0.270	4.15E-07	1.81E-06	1.38E-06	5.00E-09	0.83
M3a	n	CM	2.00E-07	9.49E-06	2.50E-07	0.02	1.51E-08	16.59	0.220	0.173	0.235	5.82E-07	2.10E-06	1.65E-06	2.20E-09	0.80
M3b	n	CM	2.00E-07	9.49E-06	2.50E-07	0.02	1.51E-08	16.59	0.220	0.173	0.235	5.82E-07	2.10E-06	1.65E-06	2.20E-09	0.80
M4	p	CA	5.80E-06	4.00E-07	2.50E-07	14.50	2.51E-06	0.10	-0.057	-0.044	0.105	9.70E-05	8.85E-06	6.78E-06	6.25E-08	0.67
M5a	n	CM	2.00E-07	9.40E-06	5.00E-07	0.02	1.52E-08	32.87	0.315	0.248	0.314	5.88E-07	3.09E-06	2.43E-06	4.43E-09	0.81
M5b	n	CM	2.00E-07	9.40E-06	5.00E-07	0.02	1.52E-08	32.87	0.315	0.248	0.314	5.88E-07	3.09E-06	2.43E-06	4.43E-09	0.81
M7	n	CA	6.30E-07	1.80E-07	2.50E-07	3.50	2.50E-06	0.10	-0.057	-0.045	0.105	9.67E-05	8.85E-06	6.96E-06	1.16E-07	0.65

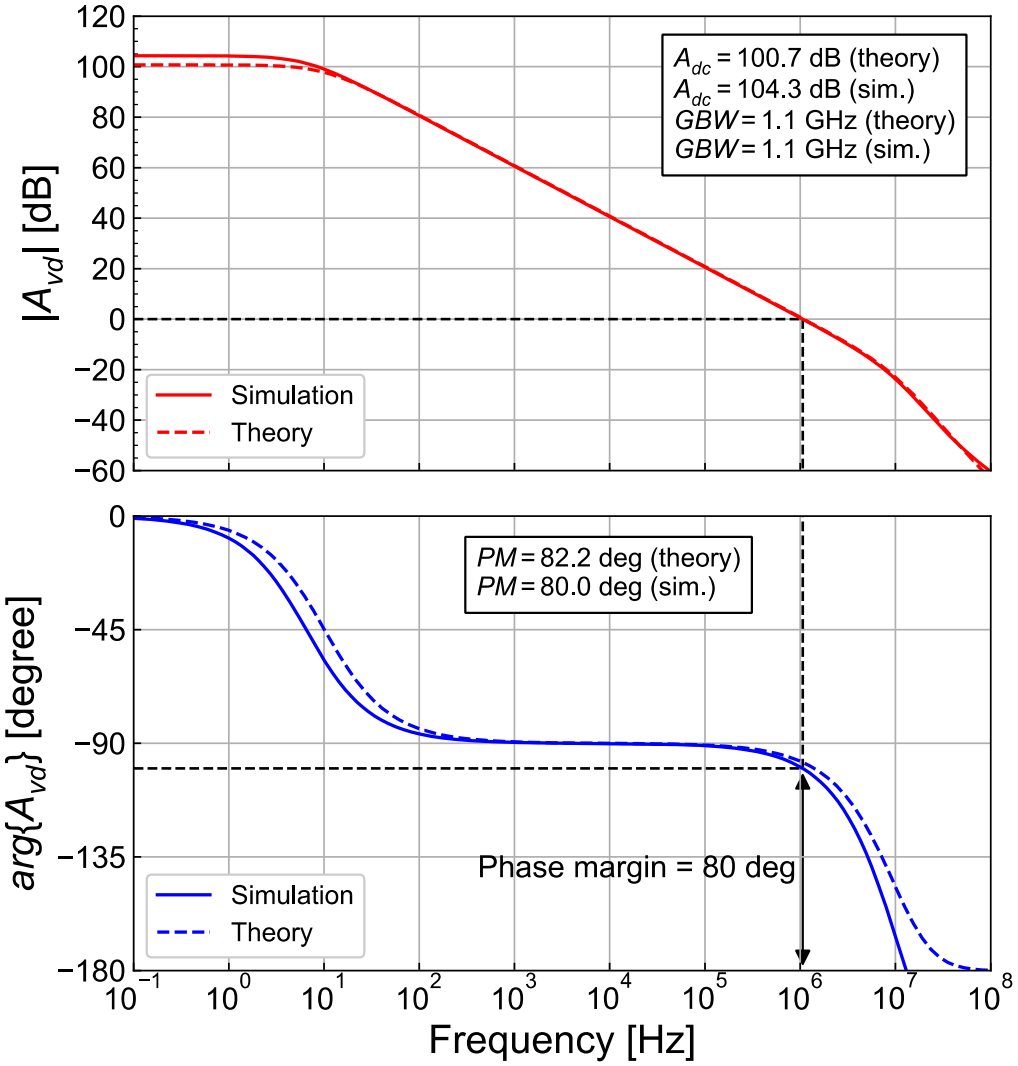
Simulations – Large-signal Transfer Characteristic



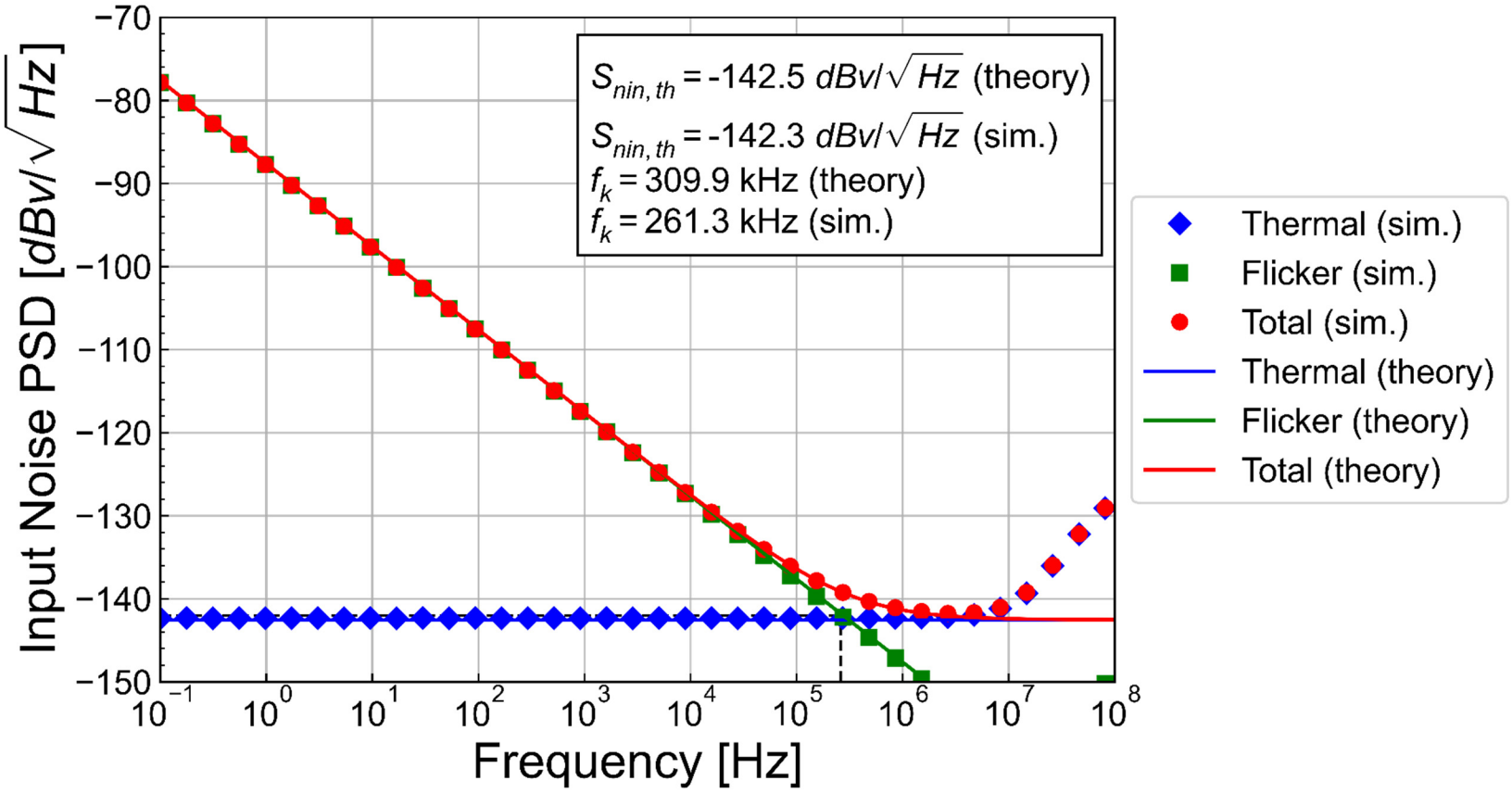
Simulations – Large-signal Transfer Characteristic (zoom)



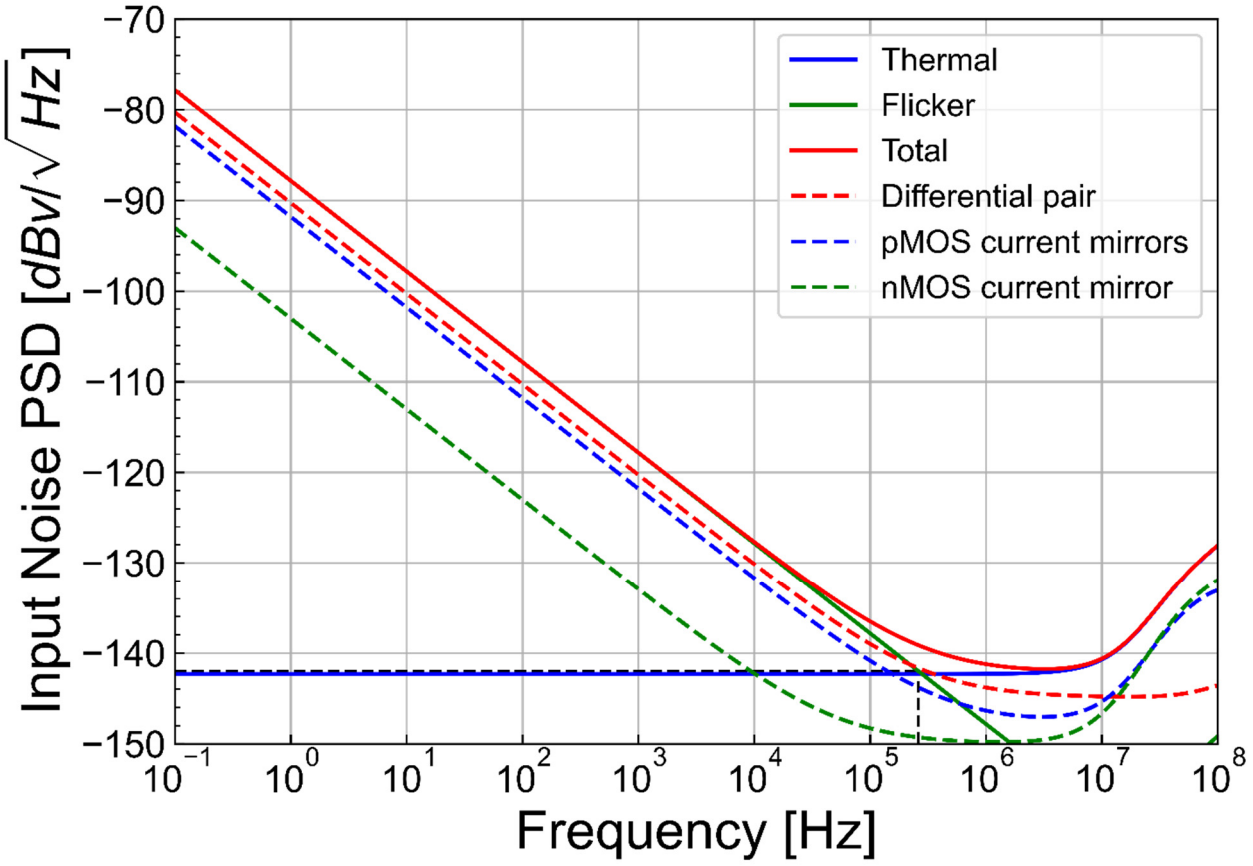
Simulations – Open-loop Gain Response



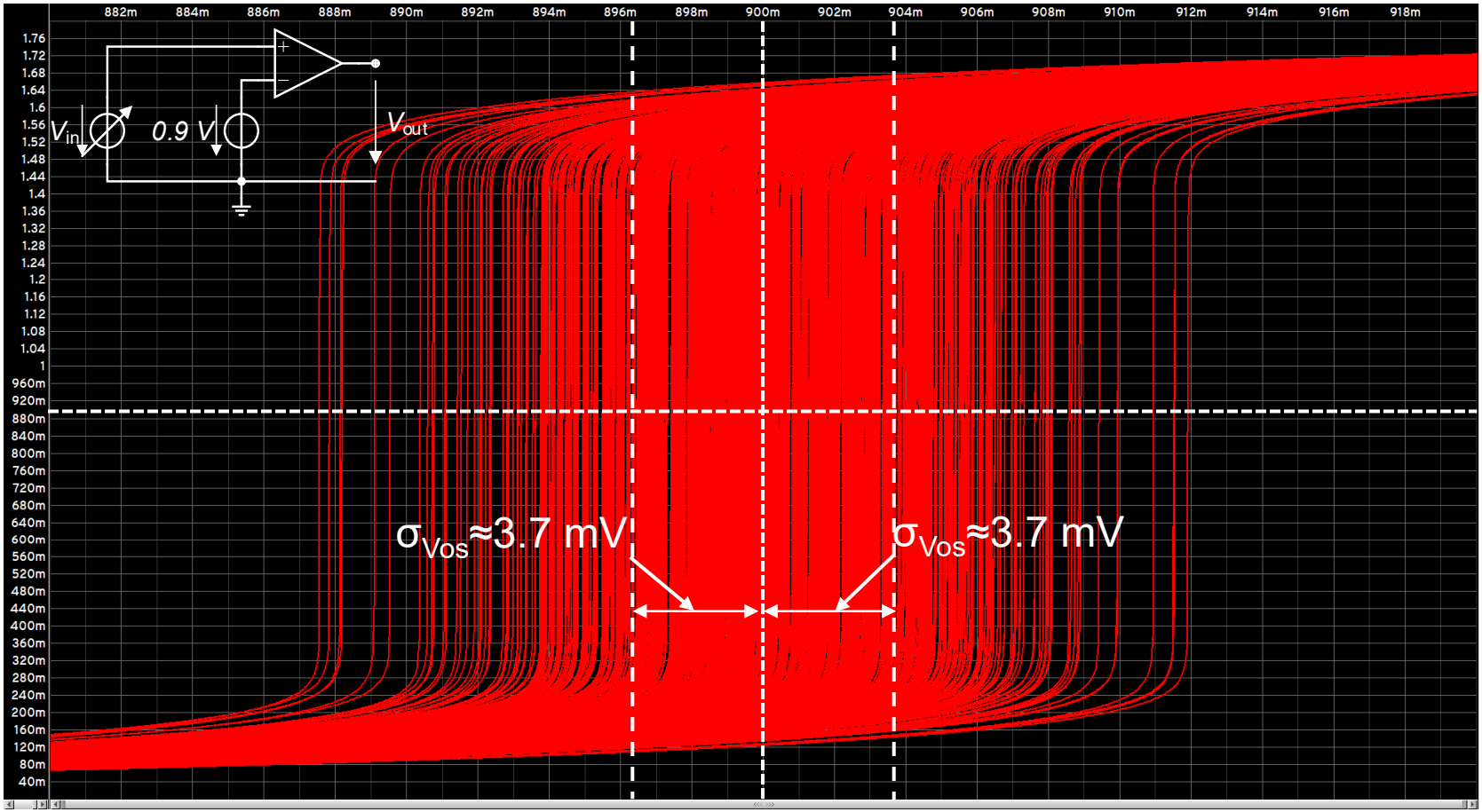
Simulations – Input-referred Noise PSD



Simulations – Individual Contributions

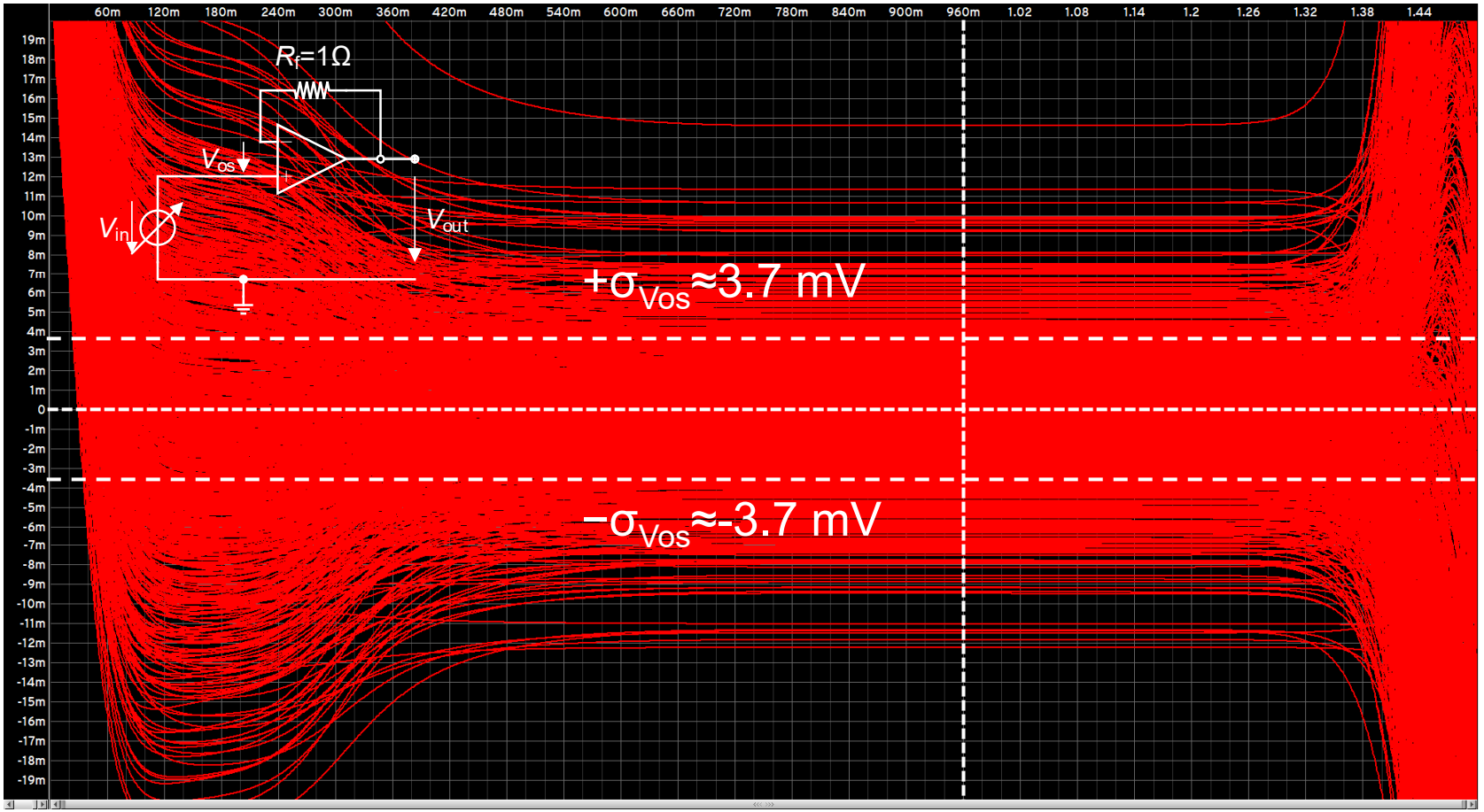


Monte Carlo Simulation of Offset Voltage (open-loop)



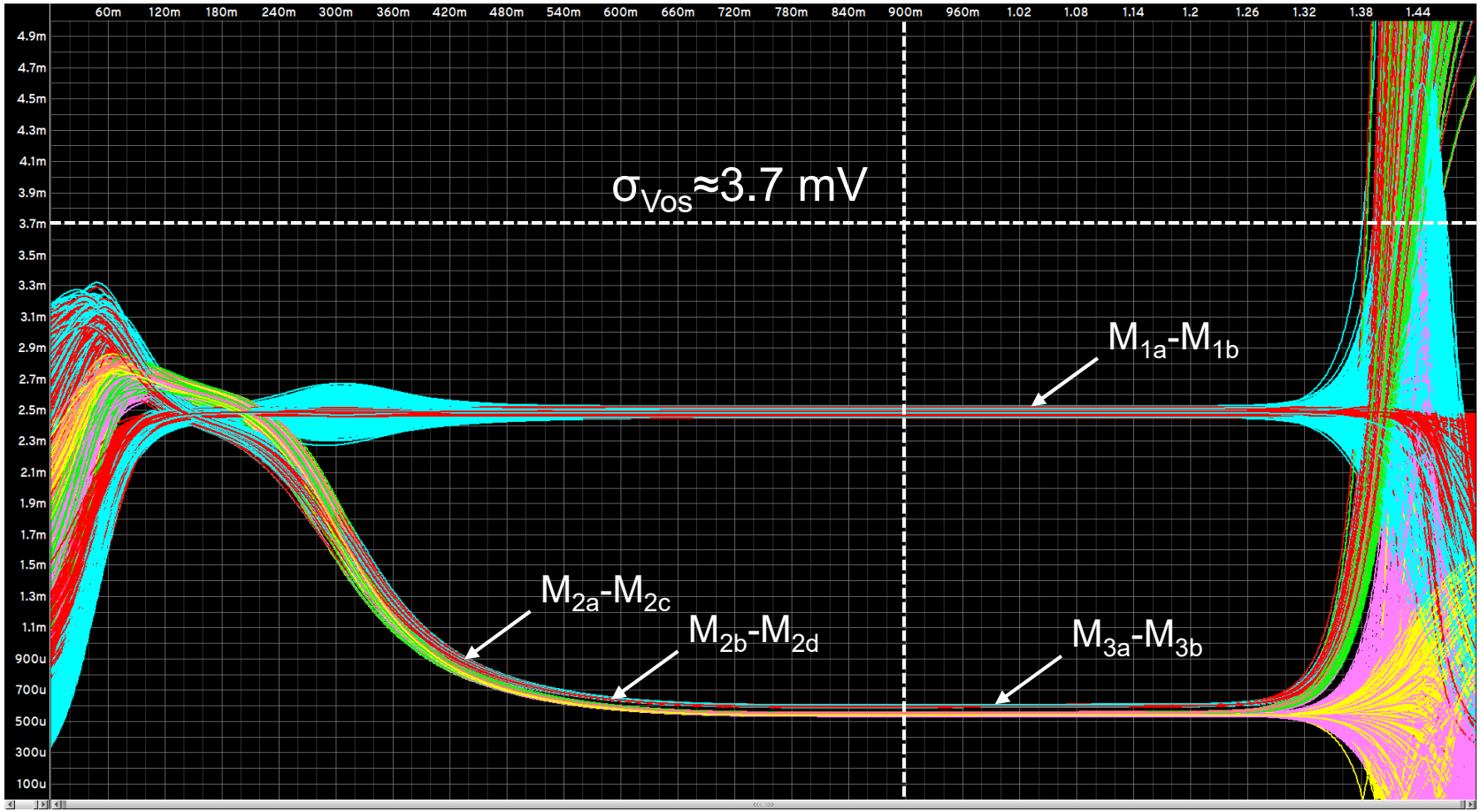
- Offset simulation using Monte Carlo simulations with 1000 runs
- The standard deviation V_{os} is about 3.73mV, which is consistent with the dispersion simulation giving 3.77 mV and close to the 3.68 mV theoretical prediction

Monte Carlo Simulation of Offset Voltage (closed-loop)



- Monte Carlo simulation of V_{os} versus V_{in} for 1000 runs in voltage follower mode
- The standard deviation of V_{os} is about 3.75 mV which is consistent with the dispersion simulation giving 3.77 mV and equal to the 3.68 mV theoretical prediction

Monte Carlo Simulation of Offset Voltage



- Offset simulation using Monte Carlo simulations with 1000 runs
- As expected the contribution of the differential pair (M_{1a}-M_{1b}) dominates within the linear range