

EE-334

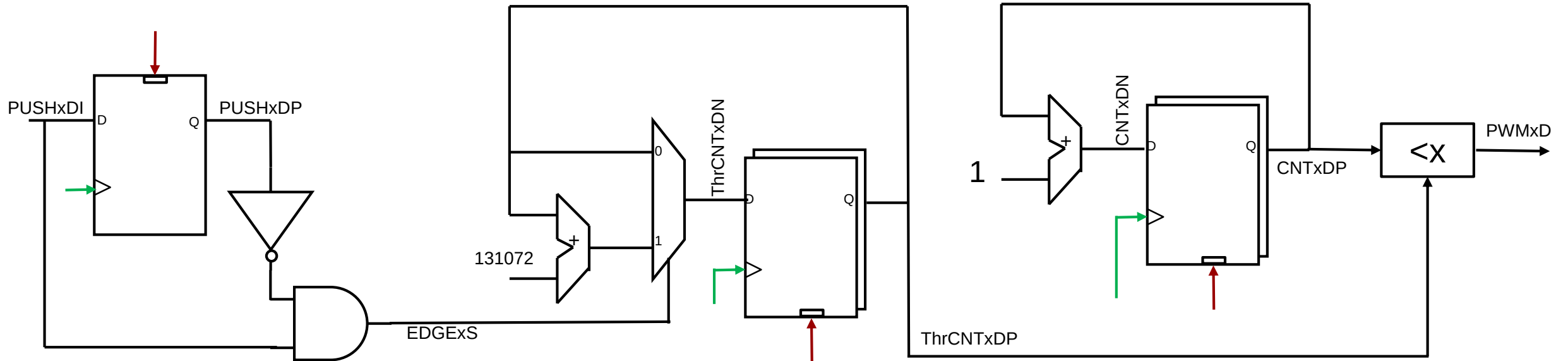
Digital System Design

Discussion for Lab 2
PWM for Color LEDs Coded in VHDL

Andreas Burg

PWM Block Diagram

- Block diagram serves as starting point for HDL coding



PWM Block Diagram

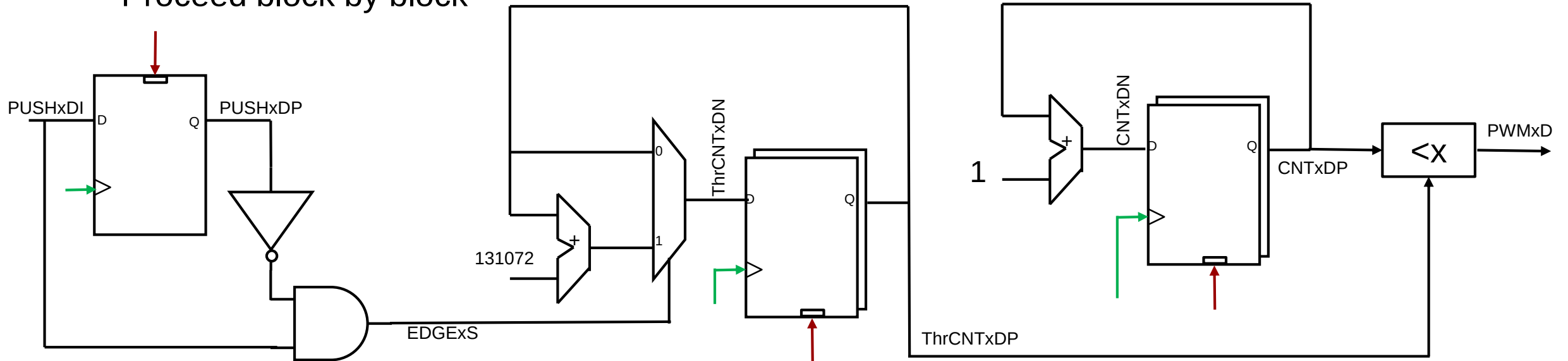
- Block diagram serves as starting point for HDL coding
 - Start with entity and signal declaration

```

entity pwm is
  port (
    CLKxCI : in std_logic;
    RSTxRI : in std_logic;
    PushxDI : in std_logic;
    LedxD0 : out std_logic
  );
end pwm;

signal EdgexSO : std_logic;
signal PushxDN, PushxDP : std_logic;
signal ThrCntxDN, ThrCntxDP : unsigned(20-1 downto 0);
signal PWMCntxDN, PWMCntxDP : unsigned(20-1 downto 0);
signal PWMxD : std_logic;
-- Edge signal
-- Push button signals (registered)
-- Threshold signals (registered)
-- PWM signals (registered)
-- PWM Pulse signal
    
```

- Proceed block by block

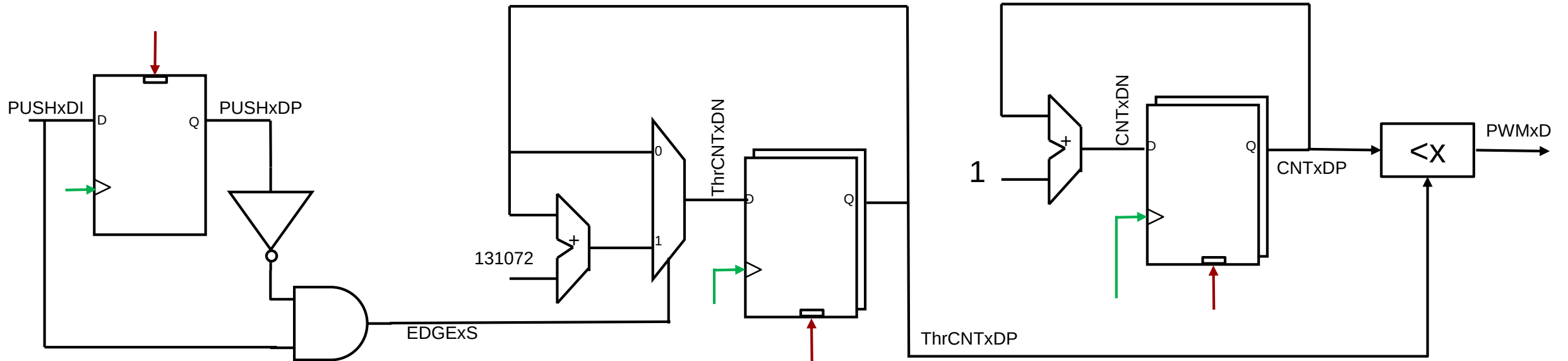


PWM Block Diagram

```
-- Edge detection
process(CLKxCI, RSTxRI)
begin
    if (RSTxRI = '1') then
        PushxDP <= '0';
    elsif CLKxCI'event and CLKxCI = '1' then
        PushxDP <= PushxDN;
    end if;
end process;

PushxDN <= PushxDI;

EdgexSO <= PushxDN and (not PushxDP);
```



PWM Block Diagram

```
-- Edge detection
process(CLKxCI, RSTxRI)
begin
    if (RSTxRI = '1') then
        PushxDP <= '0';
    elsif CLKxCI'event and CLKxCI = '1' then
        PushxDP <= PushxDN;
    end if;
end process;
```

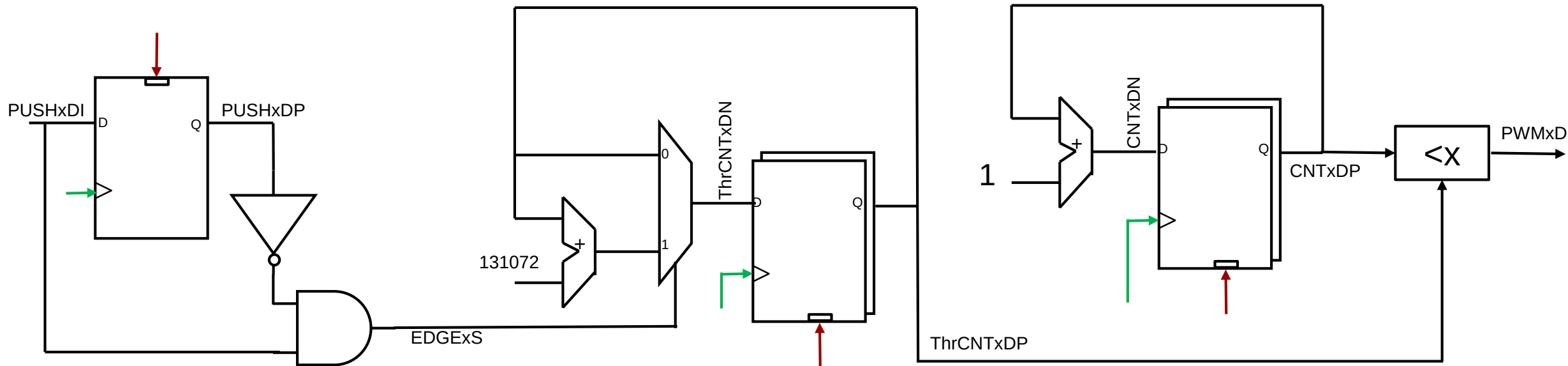
PushxDN <= PushxDI;

EdgexSO <= PushxDN and (not PushxDP);

```
-- Threshold generation
process(CLKxCI, RSTxRI)
begin
    if (RSTxRI = '1') then
        ThrCntxDN <= (others=>'0');
    elsif CLKxCI'event and CLKxCI = '1' then
        ThrCntxDN <= ThrCntxDN;
    end if;
end process;
```

-- 131072 = 2¹⁷, leading to overflow after 8

```
with EdgexSO select ThrCntxDN <=
    ThrCntxDN + 131072 when '1',
    ThrCntxDN when others;
```



PWM Block Diagram

```
-- Edge detection
process(CLKxCI, RSTxRI)
begin
    if (RSTxRI = '1') then
        PushxDP <= '0';
    elsif CLKxCI'event and CLKxCI = '1' then
        PushxDP <= PushxDN;
    end if;
end process;
```

PushxDN <= PushxDI;

EdgexSO <= PushxDN and (not PushxDP);

```
-- Threshold generation
process(CLKxCI, RSTxRI)
begin
    if (RSTxRI = '1') then
        ThrCntxDN <= (others=>'0');
    elsif CLKxCI'event and CLKxCI = '1' then
        ThrCntxDN <= ThrCntxDN;
    end if;
end process;
```

-- 131072 = 2¹⁷, leading to overflow after 8
 with EdgexSO select ThrCntxDN <= ThrCntxDN + 131072 when '1',
 ThrCntxDN when others;

```
-- PWM pulse
process(CLKxCI, RSTxRI)
begin
    if (RSTxRI = '1') then
        PWMCntxDN <= (others=>'0');
    elsif CLKxCI'event and CLKxCI = '1' then
        PWMCntxDN <= PWMCntxDN;
    end if;
end process;
```

PWMCntxDN <= PWMCntxDN + 1;
 PWMxD <= '1' when (PWMCntxDN < ThrCntxDN) else
 '0';
 LedxDN <= PWMxD;

