Timing of Synchronous Circuits

For this task, we are interested in the timing of a gate-level synchronous circuit. This analysis is typically done in detail by automatic tools, however, it is essential to understand what the tool does and what it reports. Note that we use the same principles to analyze gate level circuits and circuits at the RTL level. However, at the RTL, combinational components are usually complex sub-circuits, specified by their longest and shortest paths. In that case, we are mostly interested in a rapid (pessimistic) back-of-the-envelope estimate of the longest paths of the overall circuit. Yet, to practice the underlying foundations, in this exercise, we focus on both the longest and shortest paths to consider all timing constraints.

Hand-in instructions: Prepare a small report with your solutions (detailed). Submit your report as a PDF through the lecture moodle per the moodle submission deadline.

Terms and Concepts

Timing quantities synopsis

The timing of combinational and sequential circuits is characterized by the following quantities (see Figure 1 for an illustration):

Propagation delay t_{pd}: The time required to process new input from applying a stable logic value at a data or clock input terminal until the output has settled on its final value.

Contamination delay or **retain delay** t_{cd}: The inertial time from altering the logic value at a data or clock input until a first change of value occurs at the output. By definition, $0 \leq t_{cd} < t_{pd}$ must hold for any component or circuit.

The following timing quantities apply only to sequential sub-circuits:

Set-up time t_{su}: The lapse of time immediately before the active clock edge during which an input is required to assume a fixed logic value of either logic 0 or 1 at the input of a flip-flop. The set-up condition ensures that all nodes of a flip-flop have settled to their new values before the flip-flop locks into a new state in response to the subsequent clock edge.

Hold time t_{ho}: The lapse of time immediately after the active clock edge during which data is required to remain logically unchanged at the input of a flip-flop. The hold condition assures that all nodes of a flip-flop have settled to their new values such as to maintain that state even when the signals that caused that transitions in the first place are being removed.

The sum of t_{su} and t_{ho} is commonly referred to as data call window and often centered around the positive clock edge.

Hints and common errors

Please refer to the slides in the lecture on "Timing Analysis and Constraints in Synchronous Circuits" for the equations to check the setup and hold conditions for register-to-register, input-to-register, and output-to-register paths. The slides also contain all the necessary definitions.

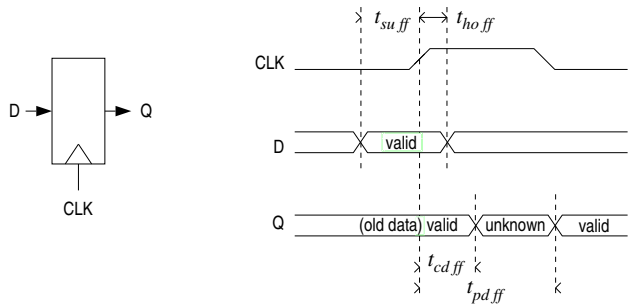

Figure 1: Positive edge triggered D flip-flop (left). Symbol and waveforms (right).

Task 1: Simple LFSR

Typical applications of shift registers are linear feedback shift registers (LFSR), which are used for generating sequences, e.g. for cyclic encoding or generating pseudo-random numbers. For example, Figure 2 shows a circuit to derive the generator polynomial for CRC4 encoding.

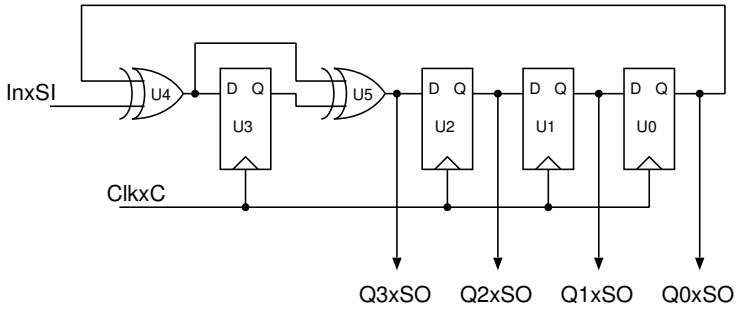

Figure 2: Cyclic coding subcircuit.

Task 1.1: Timing behavior

The propagation delays and timing requirements of the involved elements are given as follows:

- Flip-Flops (propagation and contamination delay): $t_{pd\,ff} = t_{cd\,ff} = 0.9\,\text{ns}$
- Flip-Flops (setup- and hold-time): $t_{su} = 0.5\,\text{ns}$, $t_{ho} = 0.2\,\text{ns}$
- Any logic gate (propagation and contamination delay): $t_{pd\,c} = t_{cd\,c} = 0.8\,\text{ns}$

Task 1.1a

Determine the set of signal propagation paths for the LFSR (some paths may not exist):

- Input-to-output delay: t_{io}^{min} and t_{io}^{max}.
- Input-to-register delay: t_{is}^{min} and t_{is}^{max}.
- Register-to-output delay: t_{so}^{min} and t_{so}^{max}.
- Register-to-register delay: t_{ss}^{min} and t_{ss}^{max}.

By definition, setup and hold times are not part of these delays. Remember that for any Register-to-X path you have to also consider the clock-to-Q delay of the register your path starts from. Moreover, the minimum delays are measured using contamination delays and the maximum delays are measured using propagation delays.

Task 1.1b

Explay why the minimum delays are measured using contamination delays and the maximum delays are measured using propagation delays. You may refer to the slides of the lecture.

Task 1.1c

For $t_\Delta = 0$ (the time of the stimuli application), determine the critical path, i.e., the path that limits the clock frequency. For this, you only have to consider the register-to-register and input-to-register paths. Using the critical path, determine the maximum clock speed for this sub-system.

Task 1.1d

Specify the valid time ranges for stimuli application and response acquisition at maximum speed (the speed you determined in Task 1.1b). For this, you have to derive ranges where t_T and t_Δ are valid in relation to the setup and hold conditions for the input-to-output and register-to-output paths.

Task 2: Complex LFSR

Our example is the gate-level circuit shown in Figure 3. The propagation delays and timing requirements of the involved elements are given as follows:

- Flip-Flops (propagation and contamination delay): $t_{pdff} = t_{cdff} = 0.2\,\text{ns}$
- Flip-Flops (setup- and hold-time): $t_{su} = 0.4\,\text{ns}$, $t_{ho} = 0.25\,\text{ns}$
- Any logic gate (propagation and contamination delay): $t_{pdc} = t_{cdc} = 0.1\,\text{ns}$

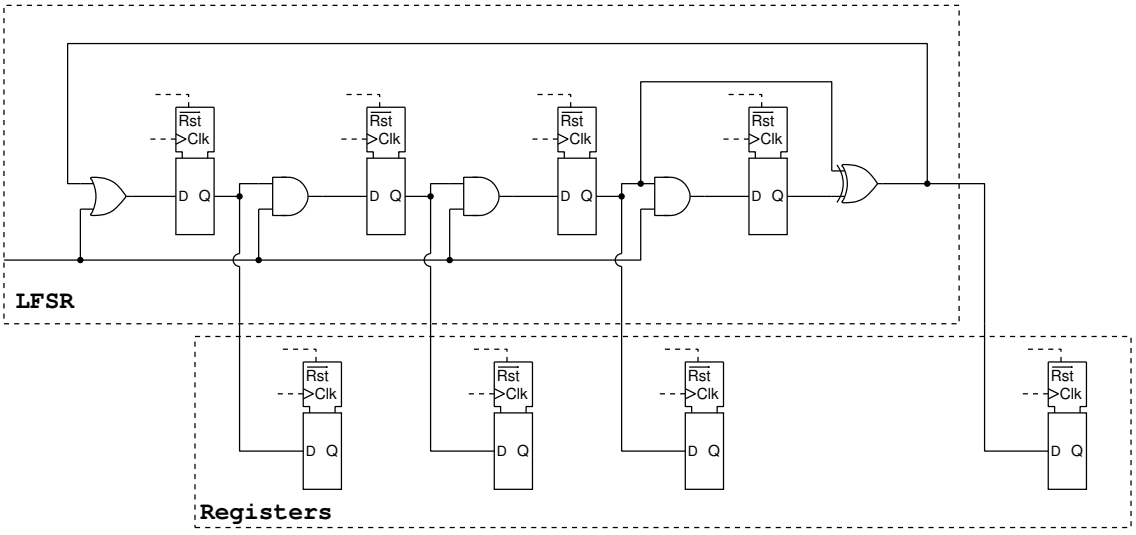

Figure 3: Gate-level schematic of an LFSR with output registers in a separate entity

Task 2.1: Minimum and Maximum Propagation Delays for Different Path Groups of the LFSR entity only

In all subtasks of Task 2.1 (2.1a - 2.1e), consider ONLY the LFSR entity. The inputs and outputs of this entity are considered as primary inputs/outputs of the overall circuit. Ignore the entity with only registers. The paths going from the LFSR entity to that entity should be considered as primary outputs.

As you know, we distinguish the following four path groups with the corresponding minimum and maximum delays:

1. Input-to-output delay: t_{io}^{min} and t_{io}^{max}.
2. Input-to-register delay: t_{is}^{min} and t_{is}^{max}.
3. Register-to-output delay: t_{so}^{min} and t_{so}^{max}.
4. Register-to-register delay: t_{ss}^{min} and t_{ss}^{max}.

Task 2.1a

Which of the four path groups is not meaningful (has no path) in the LFSR entity of the circuit shown in Figure 3?

Task 2.1b

For the three remaining path groups, specify the minimum *and* the maximum delays ($t_{??}^{min}$ and $t_{??}^{max}$). Note: by definition, setup and hold times are not part of these delays.

Task 2.1c

Assume that the stimuli application time is given by $t_\Delta = 0\,ns$. What is the minimum clock period (T_{clk}^{min}) of the circuit? Specify the corresponding condition (equation) that is used to determine this value. Clearly mark the path that determines the minimum clock period (T_{clk}^{min}) of the LFSR circuit in the figure.

Task 2.1d

Assume that the stimuli application time is now given by $t_\Delta = 0.4\,ns$. What is the minimum clock period (T_{clk}^{min}) of the circuit? Specify the corresponding condition (equation) that is used to determine this value.

Task 2.1e

Verify the hold-constraint on the LFSR entity only. Is it met?

Task 2.2: Timing of the Complete Circuit (LFSR entity together with the Registers entity)

Consider the complete circuit provided in Figure 3 for the questions below:

Task 2.2a

Mark the path in the complete circuit in Figure 3 that is the most critical for the hold-constraint (if there are multiple, one is sufficient).

Task 2.2b

Specify the equation that is used to verify the hold constraint in this figure (the equation should explicitly show the delays of all components on the relevant path).

Task 2.2c

Check the hold-constraint on the complete circuit in Figure 3. Is it met?