

EE-334

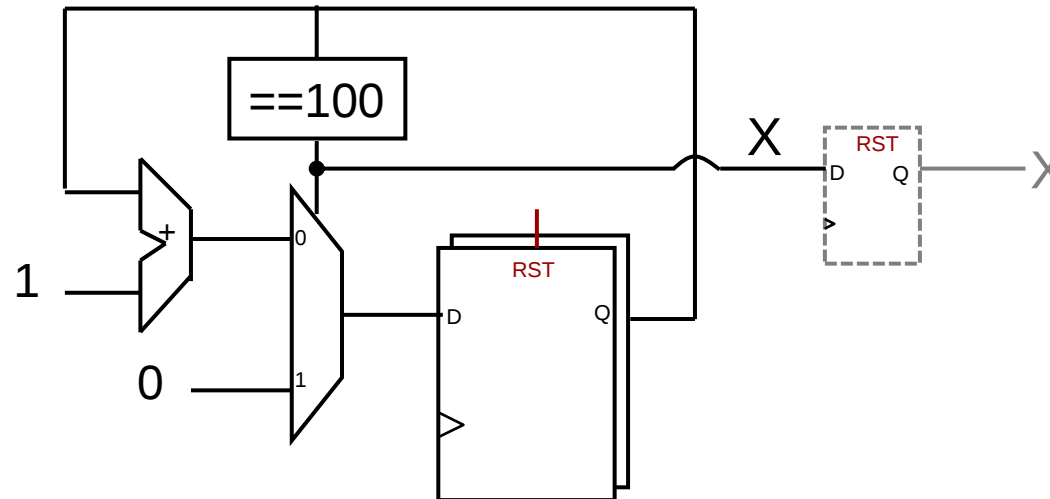
Digital System Design

Discussion for Exercise 1b
Basic RTL Design Templates

Andreas Burg

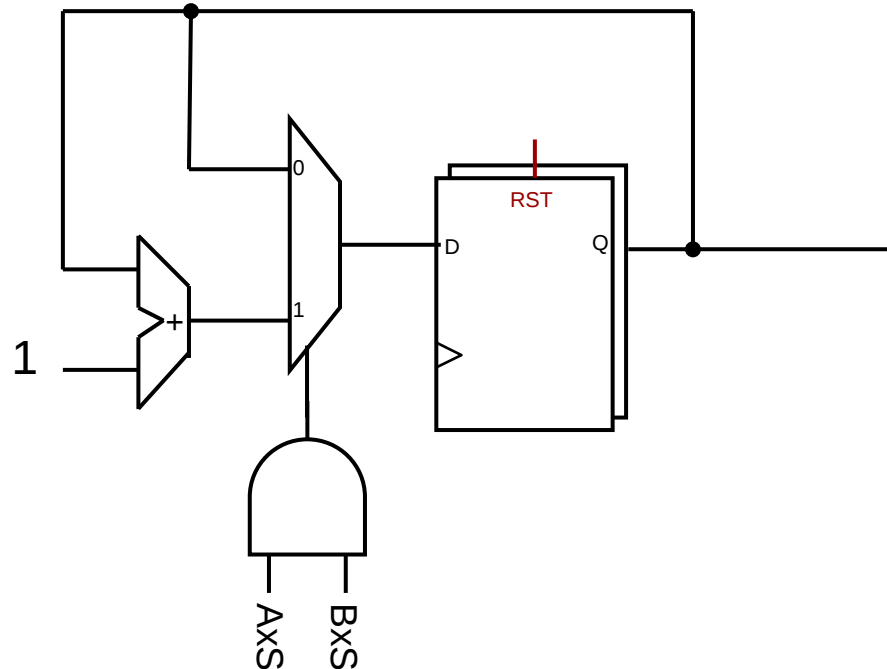
Pulse Generation

- Your block has a clock CLKxC (100 MHz=10 ns) input and an asynchronous reset RSTxR input that is only asserted once during power up and inactive (LOW) after. Implement a circuit that outputs (signal x) a 10 ns pulse ('1') every microsecond (every 100 cycles).



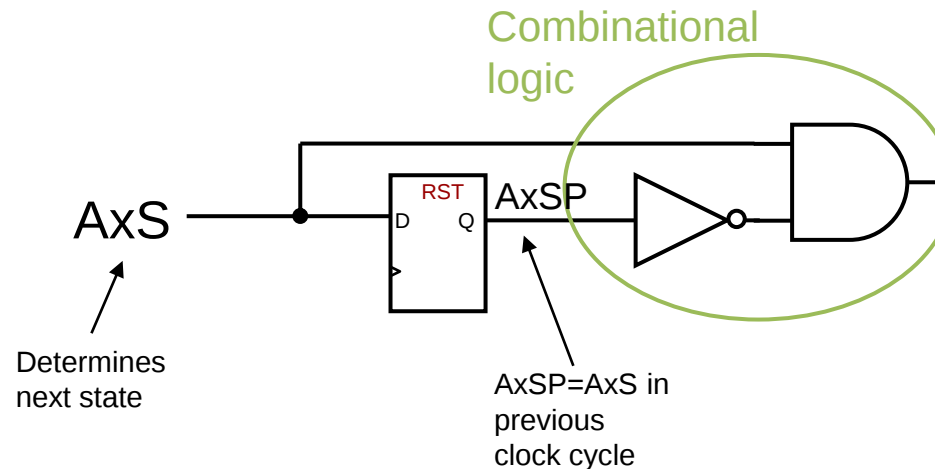
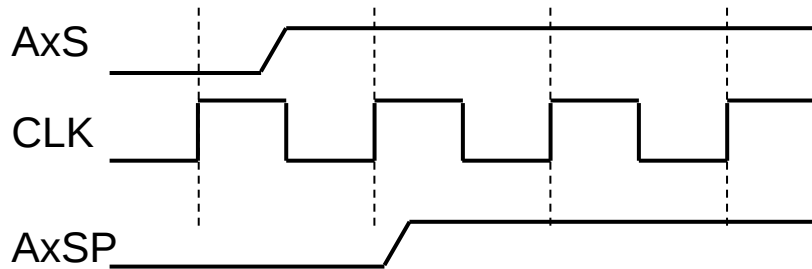
Count up with conditional enable

- The input of your block are two 1-bit signals AxS and BxS as well as a clock $CLKxC$ and an asynchronous reset $RSTxR$ that is only asserted once during power up and inactive (LOW) after. Count and output the number of clock cycles in which both inputs are '1'.



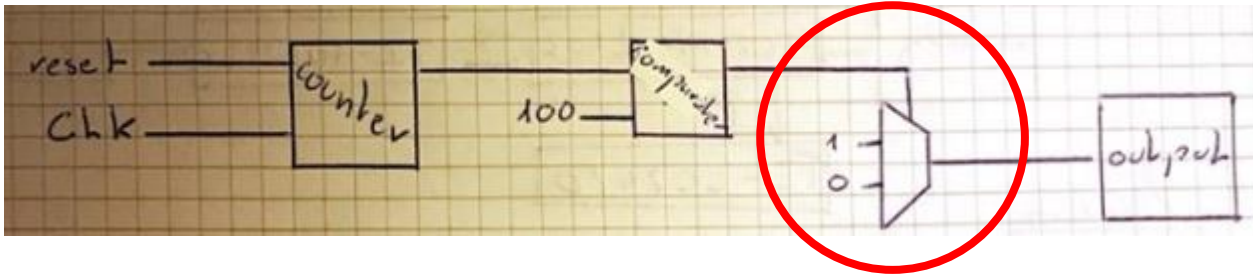
Edge Detector

- The input of your block is a 1-bit signals AxS as well as a clock $CLKxC$ and an asynchronous reset $RSTxR$ that is only asserted once during power up and inactive (LOW) after. The signal AxS can change from '0' to '1' and from '1' to '0' at random moments in time. Implement a circuit that outputs (signal x) a '1' for only a single clock cycle every time the input transitions from '0' to '1'.

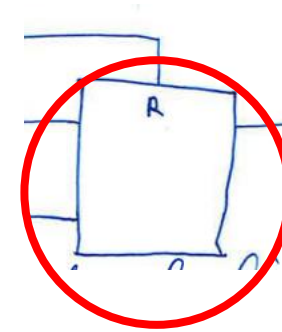


Common Mistakes 2022: small stuff

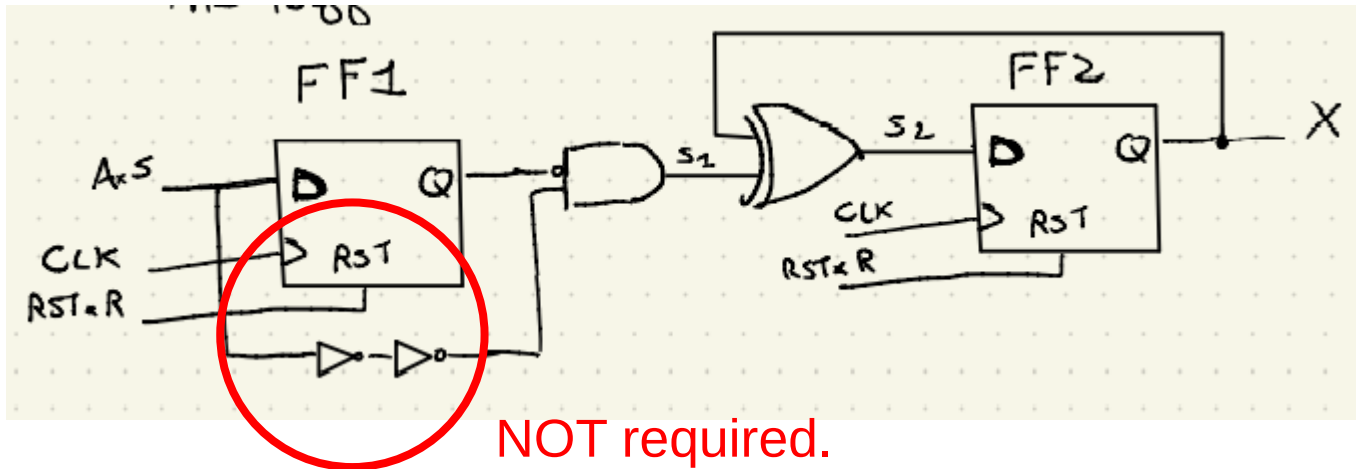
- Slightly too complicated or too complex or unclear



What is this for?



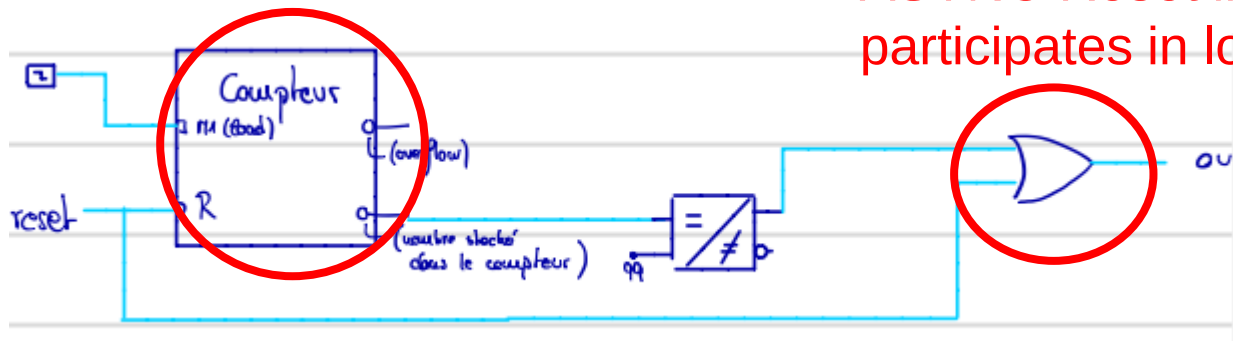
This may be a FF, but which input is which?



NOT required.

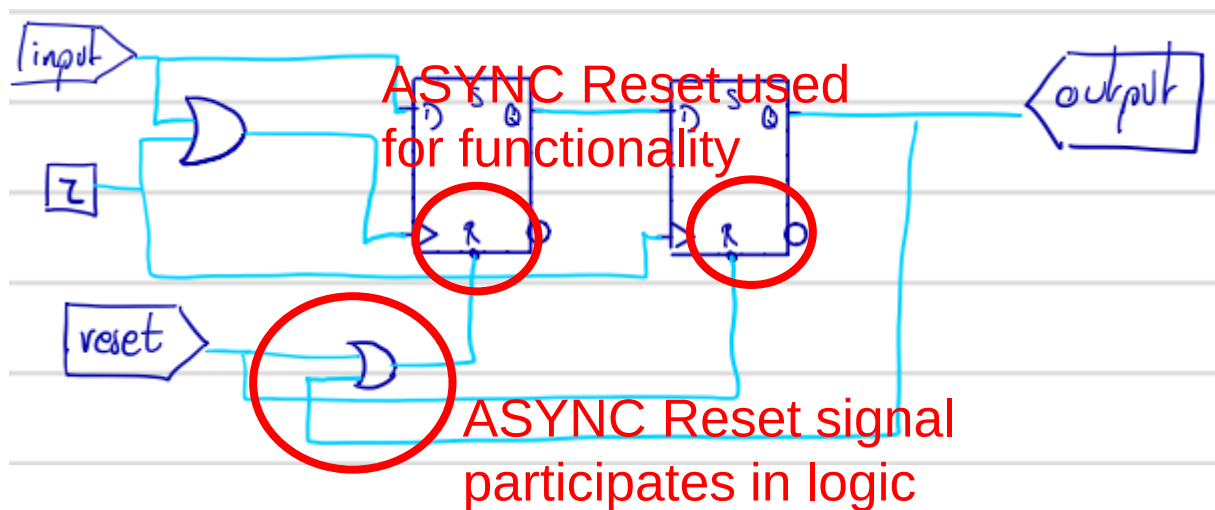
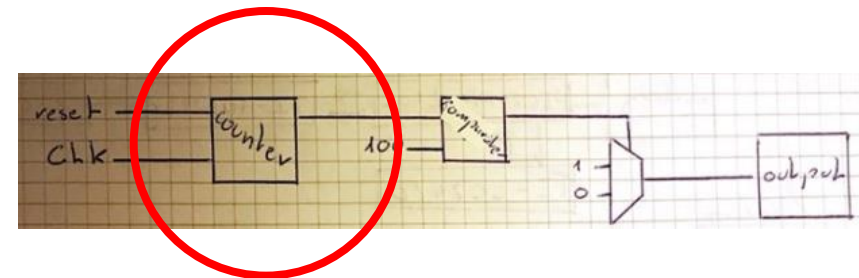
Common Mistakes 2022: bad stuff

Too much abstracted: what is inside?



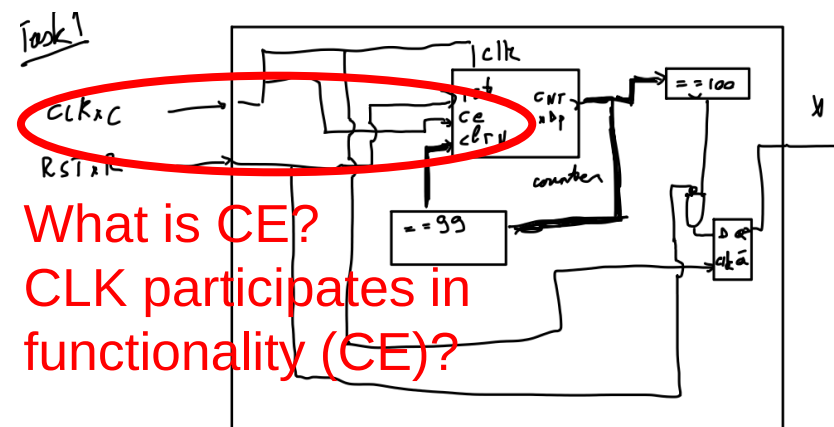
ASync Reset input participates in logic

Too much abstracted:
what is inside?



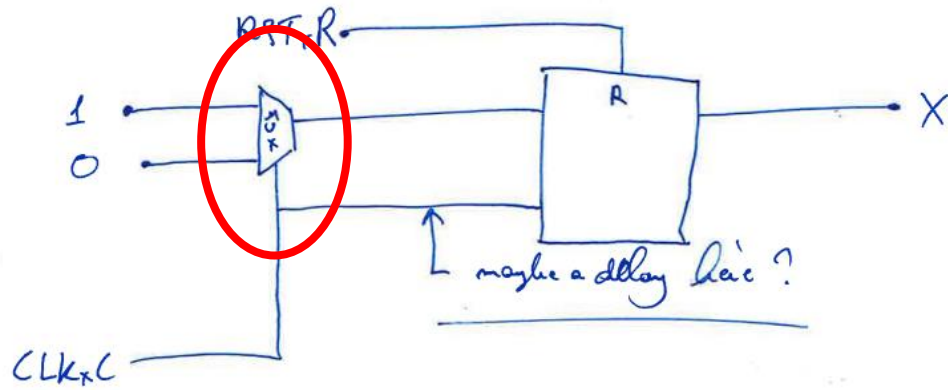
ASYNC Reset used for functionality

ASYNC Reset signal
participates in logic

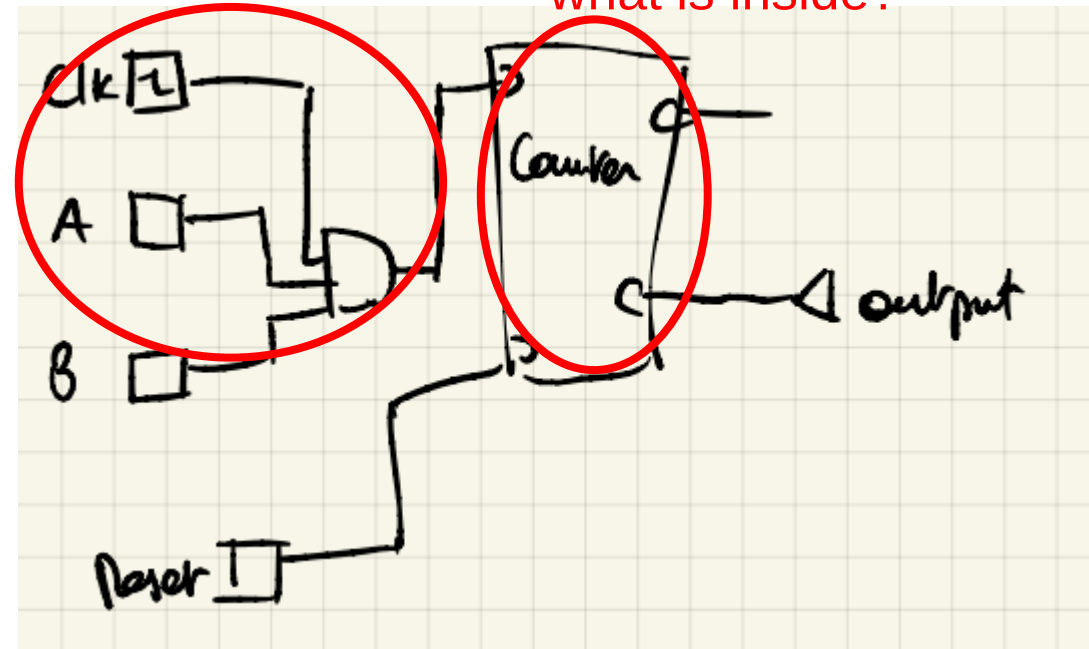


What is CE?
CLK participates in
functionality (CE)?

Common Mistakes 2022: bad stuff

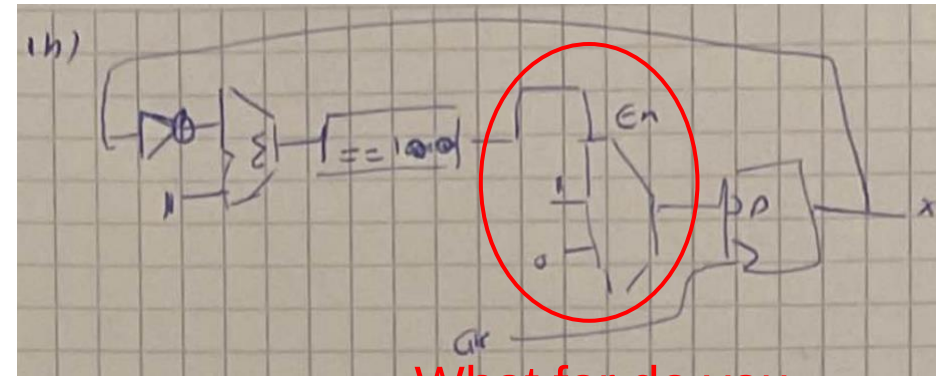
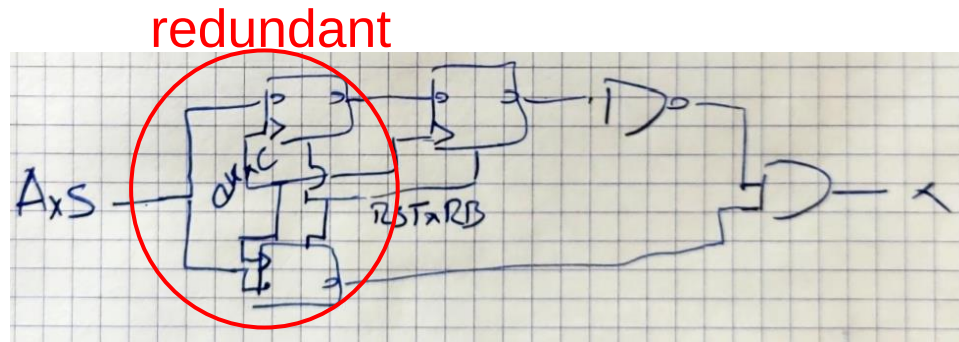


Too much abstracted:
what is inside?

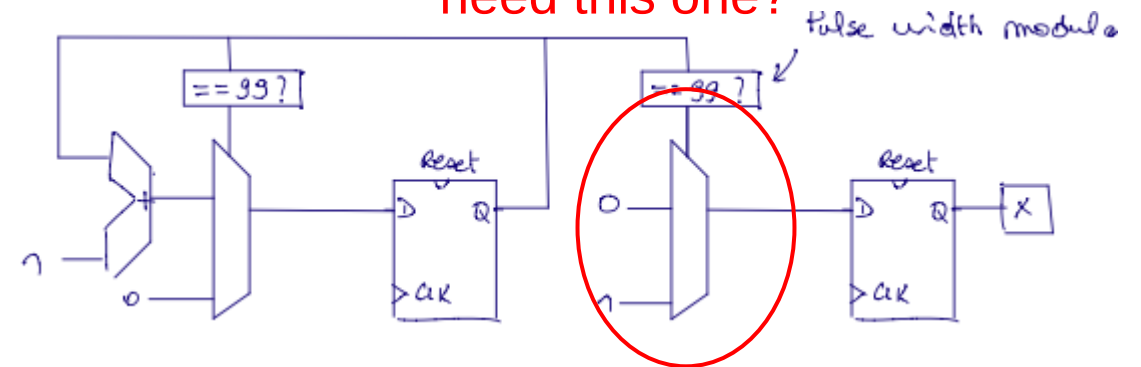
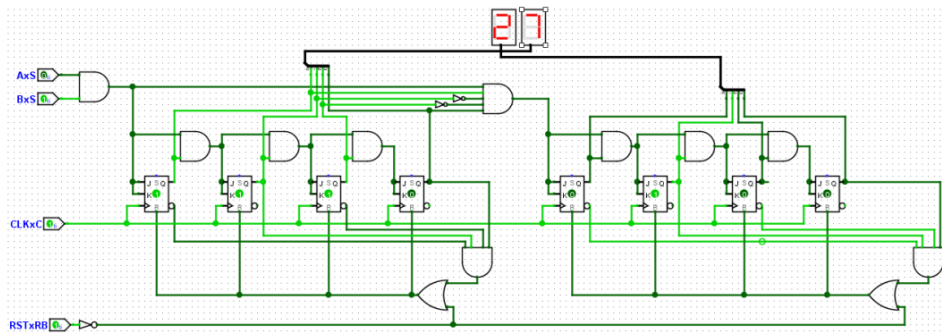


Common Mistakes 2021: small stuff

- Slightly too complicated or too complex



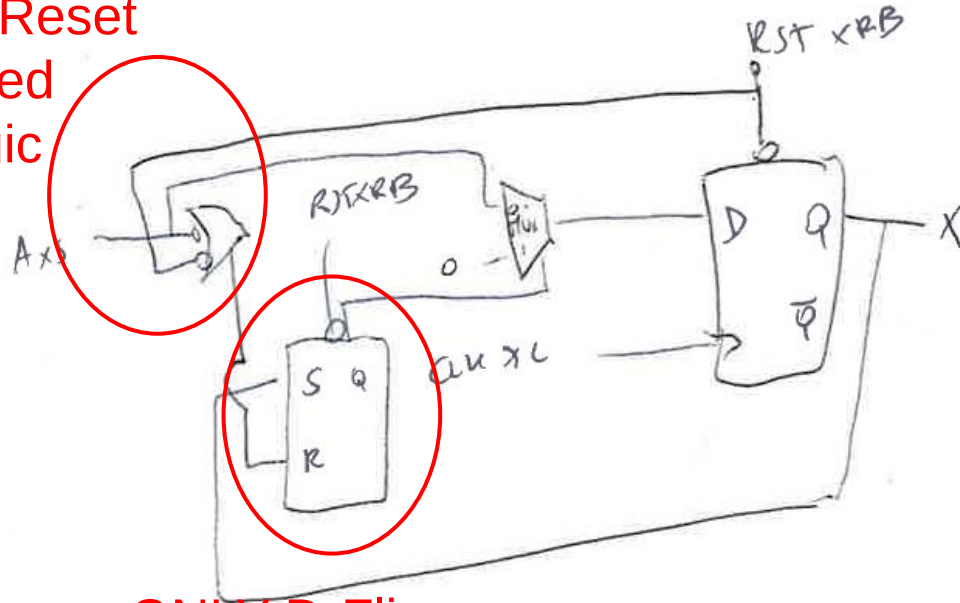
What for do you need this one?



Don't make your life complicated.
This is not a logic design class. Abstract

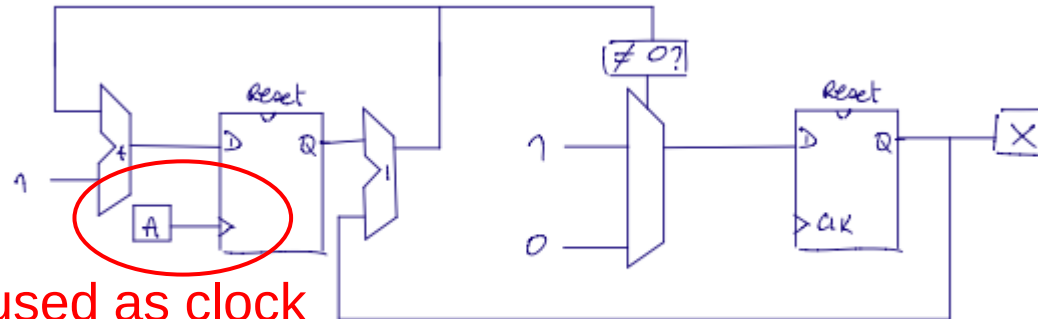
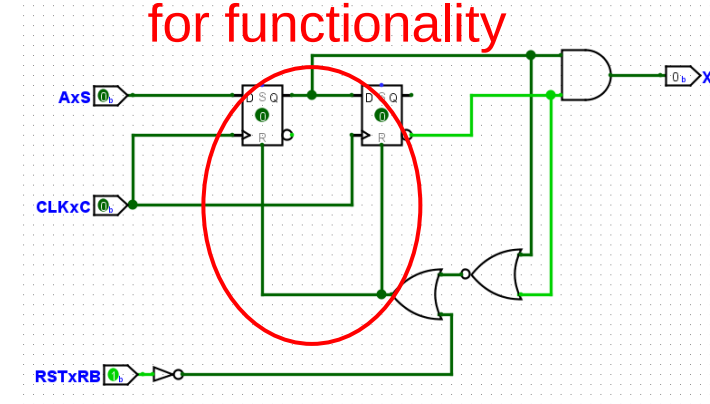
Common Mistakes 2021: bad stuff

Async. Reset
combined
with logic



ONLY D-Flip
Flops

Async. Reset used
for functionality



Data/inputs used as clock