THEORY CLASS (ONLINE) VHDL LANGUAGE CLASS (ONLINE) **LAB/EXERCISE SESSION**

Wk	Date	Room	Time	Content
1	11 Sep		8h15 – 11h00 11h15 – 12h00	Organization of the Course Introduction to Digital Systems and Components Fundamentals of Synchronous Design Exercises: System Level Design & RTL Design Basics (drawing block diagrams)
2	18 Sep		8h15 – 09h00 9h15 – 10h00 10h15 – 12h00	FPGA Background Introduction to VHDL: HDLs, MODELING & DESIGN, HDL-based Design Flow VHDL for RTL Design and Synthesis (Fundamental Structure) & Packages Vivado Tutorial: get to know the tools
3	25 Sep		8h15 – 11h00 8h15 – 12h00	VHDL for Synthesis (Part 1): Concurrent statements More VHDL for Synthesis: (Part 2) Processes and Sequential Statements Exercise: Block Diagram of PWM Controller
4	02 Oct		8h15 – 12h00	RTL to VHDL and Vice-Versa VHDL Introductory example: PWM Controller
5	09 Oct		8h15 – 10h00 10h15 – 11h00 11h15 – 12h00	Finite State Machines VHDL for Simulation and Testbenches (Timing of Synchronous Circuits) – time permitting Exercise (preparation): Finite State Machine on paper: Door Lock
6	16 Oct		8h15 – 10h00 10h15-12h00	Timing of Synchronous Circuits From Algorithms to Architecture (Part 1) Exercise on Static Timing Analysis
	23 Oct	VACATION		
7	30 Nov		08h15 – 12h00	FSMs in VHDL: Door Lock RTL & Testbenches
8	06 Nov		8h15 -10h00 10h15 – 12h00	From Algorithms to Architecture (Part 2) Fixed Point Arithmetic and Datapath in VHDL Exercise from Algorithms to Architectures using Mandelbrot
9	13 Oct		08h15 – 12h00	Exercise: Lab on Simulating and Debugging VHDL
10	20 Nov		8h15 – 9h00 9h15 – 12h00	Project Intro, Video Interface & VGA Project: VGA Interface
11	27 Nov		8h15 – 12h00	Project: Pong (Video Memory & Pong Game)
12	04 Dec		8h15 – 10h00 8h15 – 12h00	Mandelbrot Data Paths Project: Pong (Mandelbrot)
13	11 Dec		8h15 – 12h00	Project: Pong
14	18 Dec		8h15 – 12h00	Project: Pong PRESENTATIONS