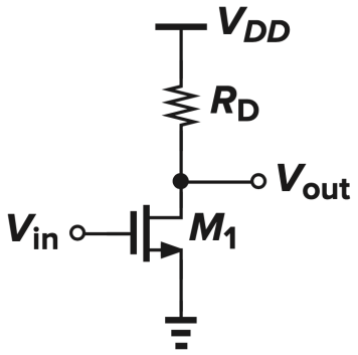
EE-320 Exercise 7

1. Design a common-source amplifier with a resistive load (schematic shown below) with the following design specifications. Assume $\lambda=0$, $\gamma=0$, $V_{DD}=3V$, $V_{TH}=0.5V$, $\mu_n C_{ox}=1mA/V^2$.

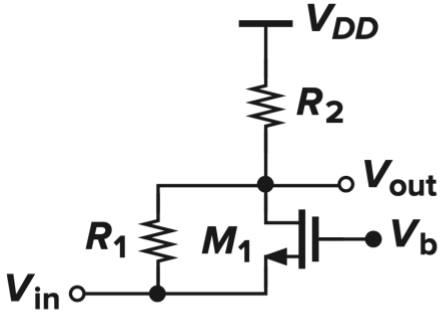
- M_1 is in saturation
- The minimum output voltage to keep M_1 in saturation is 0.2V
- The total power consumption of the amplifier is 3mW
- The absolute value of gain is 15
- L=0.5µm for the transistor



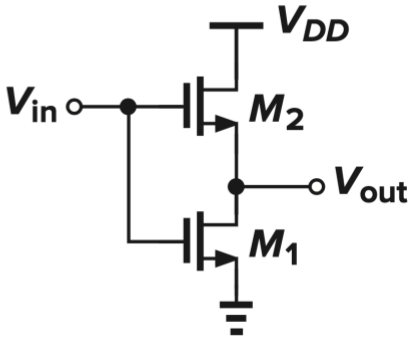
Find the following:

a) DC level of the input
b) The width (W) of M_1
c) R_D
d) DC (bias) level of the output

2. Assuming transistors are in saturation, calculate the small-signal voltage gain of the following circuits ($\lambda\neq0$, $\gamma=0$).



(a)



(b)