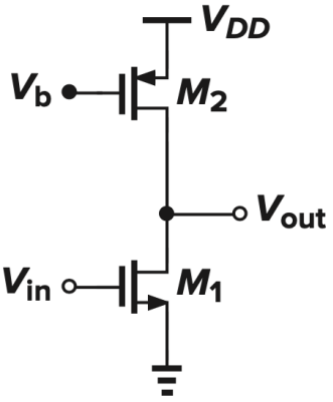
EE-320 Exercise 5

1. In the circuit shown below, assume that $(W/L)_1 = 50/0.5$, $(W/L)_2 = 50/2$, and $I_{D1} = I_{D2} = 0.5$ mA and both devices are in saturation. Calculate the small-signal voltage gain. Assume $\mu_n C_{ox} = 0.134$ mA/V^2, $\mu_p C_{ox} = 0.038$ mA/V^2, λ=0.1 for NMOS, λ=0.2 for PMOS, the bulk of PMOS is connected to V_{DD} and the bulk of NMOS to GND.



2. Consider the following CS stage with a diode-connected load, $(W/L)_1 = 50/0.5$ and $(W/L)_2 = 10/0.5$. Assume that $\lambda = \gamma = 0$. At what input voltage is M_1 at the edge of the triode region? What is the small-signal gain under this condition? Assume $V_{TH0} = 0.7$ V and $V_{DD} = 3$ V.