The buttons, joystick, and dip-switches can either be used in polling-mode or in interrupt-based mode. The base-address of this interface is `0x50000080`. The different functions are shown below:

byte index	word index	Functionality:	
		read:	**write:**
0	0	Read the dip-switches state	No operation
4	1	Read and clear pressed dip-switch IRQ generators	Write dip-switch pressed IRQ enable mask
8	2	Read and clear released dip-switch IRQ generators	Write dip-switch released IRQ enable mask
12	3	Read the joystick and buttons state	No operation
16	4	Read and clear pressed joystick and buttons IRQ generators	Write joystick and buttons pressed IRQ enable mask
20	5	Read and clear released joystick and buttons IRQ generators	Write joystick and buttons released IRQ enable mask
24	6	Read IRQ latency value	No operation
28	7	Clear all IRQ generators	Clear all IRQ enable masks

When addressing the dip-switches, the bit 0 of the 16-bit word corresponds to the dip-switch to the right (nr. 8) of the board. Bit 15 of the 16-bit word corresponds to the dip-switch to the left (nr. 1) of the board in case of the GECKO4Education. In case of the GECKO5Education only the lower 8 bits are available, all others read 0. This coding also holds for the IRQ-masks and IRQ-generators. When addressing the buttons, the GECKO4Education and GECKO5Education have different mappings:

- **GECKO4Education** : the button SW2 (see also the gecko-wiki) is mapped on the LSB, and SW7 is mapped on bit 5.
- **GECKO5Education** : the button SW1 is mapped on bit 5 and SW5 on bit 9. The joystick is mapped as shown below:

bit nr.	Joystick function:	bit nr.	Joystick function:
3	North	2	East
1	South	0	West
4	Center button	-	-

These coding also holds for the IRQ-masks and IRQ-generators.

1 Scanning frequency

The buttons, joystick, and dip-switches are scanned to avoid any dender effects. The standard frequency of this scanning is 1kHz.

2 IRQ handling

Interrupts can be enabled for both pressing a button or releasing a button. The interrupts are enabled in the pressed or released IRQ enable masks. In case an interrupt is enabled and a corresponding action is detected (press and/or release) an interrupt is generated. The dip-switches will activate `IRQ bit2`, the joystick, and buttons will activate `IRQ bit3` of the user-CPU. To see to sources of the IRQ, the pressed and/or released IRQ generators registers can be read out. Reading these registers will then automatically clear the IRQ-event. If a user want to clear all sources that generated an IRQ, a read of the `Clear all IRQ generators` register can be performed. To clear all IRQ-enable masks a write to the `Clear all IRQ enable masks` register can be performed.
Finally, the IRQ's generated by the module are active-high and stay active up to the moment the CPU clears the IRQ-generators by the means described above.

3 IRQ latency counter

The module also implements a 32-bit latency counter. This counter will count the number of system clock cycles between the moment an IRQ is generated and it is cleared by the CPU.