Design Technologies for Integrated Systems – EPFL

Midterm Exam **26/10/2023**

NAME and SURNAME (in capital letters):

No. SCIPER:

Problem 1: _____/15. – Boolean Algebra

Problem 2: _____/30. – Scheduling

Problem 3: _____/15. – Resource Sharing

Problem 4: _____/25. – Two-Level Logic Optimization

Problem 5: _____/25. – Behavioral-Level Optimization

Problem 6: _____/10. – Boolean Operators

Total: _____/120

Problem 1 – (15 pts)

Given the Boolean function f:

$$f = a \wedge b \wedge c$$

(a) Show the minimum implementation of Boolean negation, constant zero, and constant one using only two-input NORs. The formula should not contain any constant. (5 pts)

(b) Find a formula equivalent to f that uses only two-input NORs. The formula should not contain any constant and should be as short as possible (minimum number of NORs and literals). (10 pts)

Solution to Problem 1 (a)

- Boolean negation ($\bar{a}$) :

- Constant zero ($\perp$) :

- Constant one ($\top$) :

Solution to Problem 1 (b)

$f =$

Number of 2-input NORs in the formula = _____.

Number of literals in the formula = _____.

Problem 2 – (30 pts)

For all sub-questions in Problem 2, consider the following sequencing graph:

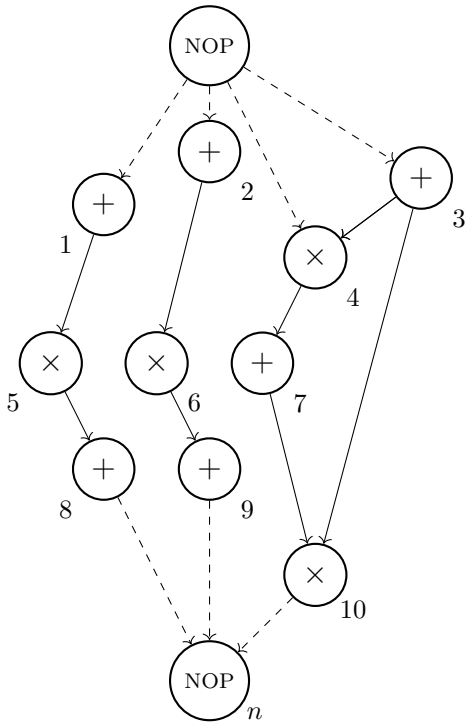


Figure 1: Sequencing graph for Problem 2.

For problems (a) and (b), assume all operations take unit delay and there is no resource constraint.

(a) Schedule Figure 1 with ASAP (0 pts; i.e. no need to show); what is the smallest latency of this sequencing graph? (3 pts)

(b) Schedule Figure 1 with ALAP using the latency λ obtained in (a) as the latency upper bound $\bar{\lambda}$ (0 pts; i.e. no need to show); then use the scheduling graphs to compute the mobility (slack) of each operation. (5 pts)

For problems (c), (d), and (e), assume that adders take 1 unit of delay and multipliers take 2 units of delay. Assume that operations of the same type which do not operate at the same time share the resource.

(c) Schedule Figure 1 using the list scheduling algorithm to minimize the latency subject to the resource constraint of at most 2 adders and 1 multiplier. (5 pts) What is the obtained latency subject to resource constraints? (1 pt)

(d) Assuming a maximum latency of 6, use the list scheduling algorithm to minimize the resources. (10 pts) How many of each type of resource are used? (2 pts)

(e) Assuming a maximum latency of 6, would it be possible to have a scheduling with a smaller number of resources than that given by list scheduling? If so, how many adders and multipliers are sufficient? (4 pts)

Solution to Problem 2 (a)

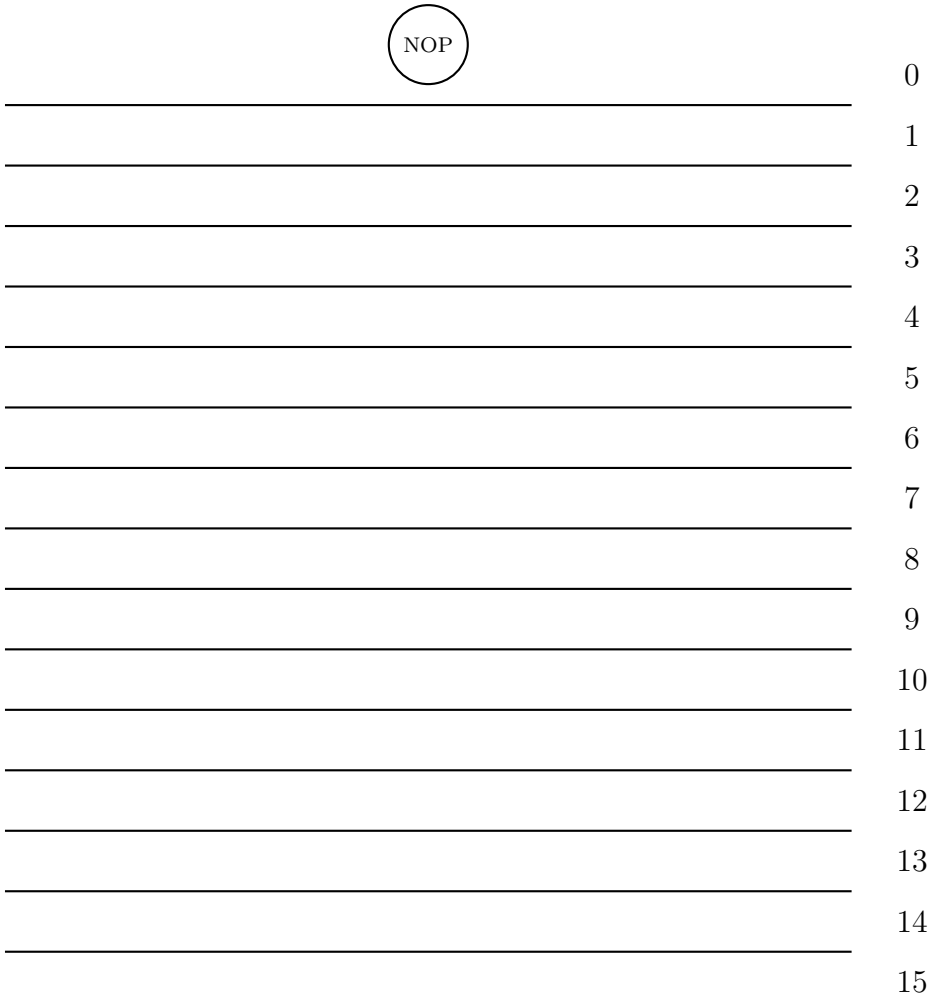
The smallest latency is $\lambda =$ _____.

Solution to Problem 2 (b)

	v_1	v_2	v_3	v_4	v_5	v_6	v_7	v_8	v_9	v_{10}
$\mu = t_L - t_S$										

Solution to Problem 2 (c)

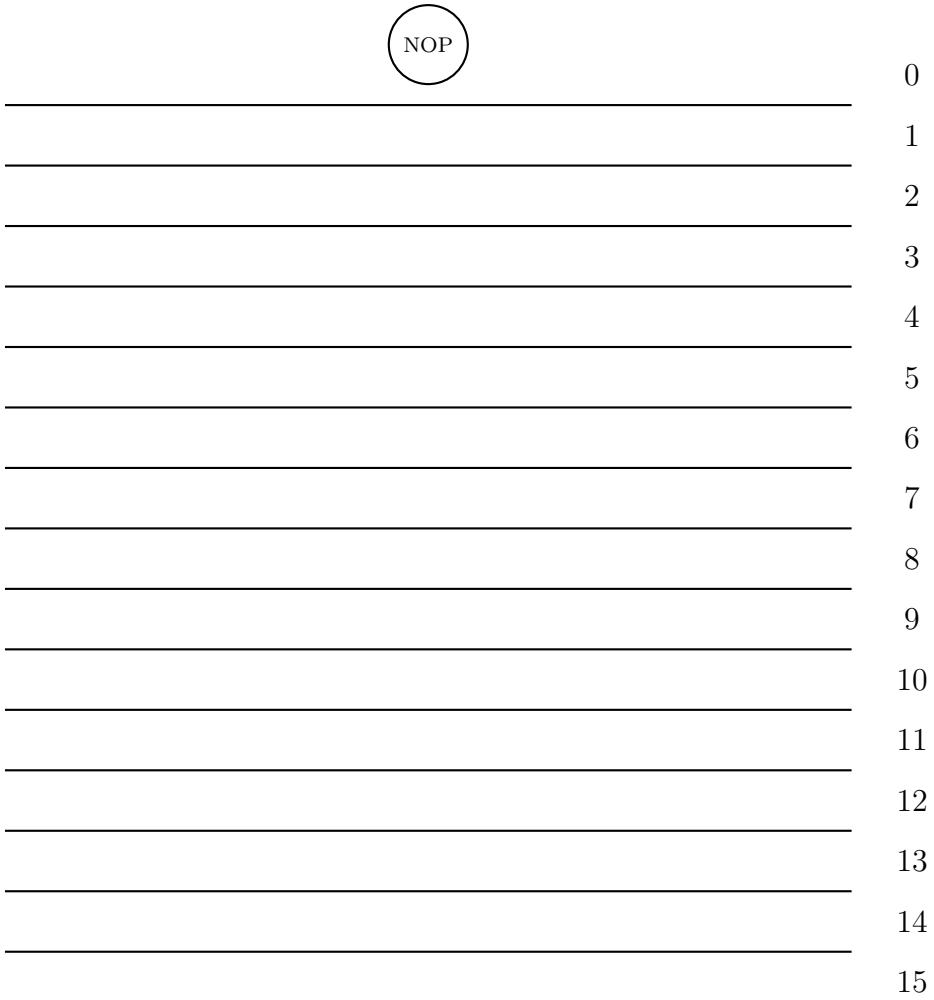
Please mark the indices of each operation.



The obtained latency is $\lambda =$ _____.

Solution to Problem 2 (d)

Please mark the indices of each operation.



Number of adders: _____. Number of multipliers: _____.

Solution to Problem 2 (e)

Is it be possible to have a scheduling with a smaller number of resources than that given by list scheduling? _____.
Number of adders: _____. Number of multipliers: _____.

Problem 3 – (15 pts)

Given the scheduled graph in Figure 2.

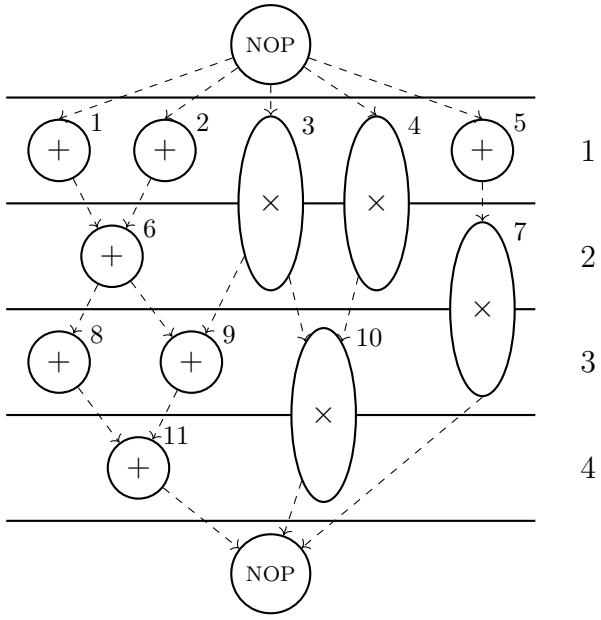


Figure 2: Scheduled graph for Problem 3.

(a) Draw the conflict graphs for the multiplier and adder operations. (5 pts)

(b) Determine the minimum number of resources for the multiplier and adder by using the left-edge algorithm. Show the coloring steps as a conflict graphs represented using intervals. (10 pts)

Solution to Problem 3 (a)

Solution to Problem 3 (b)

Problem 4 – (25 pts)

Given the Boolean function f:

$$f = abd + \bar{a}b\bar{d} + \bar{a}\bar{b}\bar{d} + \bar{b}cd + b\bar{c}d + \bar{b}c\bar{d} + b\bar{c}\bar{d}$$

(a) Draw the minterms on the hypercube shown in Figure 3. (*Hint: There are 11 minterms!*) (5 pts)

(b) List all the primes for f. (5 pts)

(c) List all the essential primes for f. (6 pts)

(d) Find a minimum cover for f. (4 pts)

(e) Assuming that the function value is irrelevant (i.e., the output is not observed by the environment) for the input combination $a = 0$, $b = 1$, $c = 1$, $d = 1$ and $a = 1$, $b = 1$, $c = 1$, $d = 0$ (these two input combinations are *don't care terms*), obtain a simplified cover for f. Namely, for these input combinations, you can change the function value as you wish such that it helps the simplification. (5 pts)

Solution to Problem 4 (a)

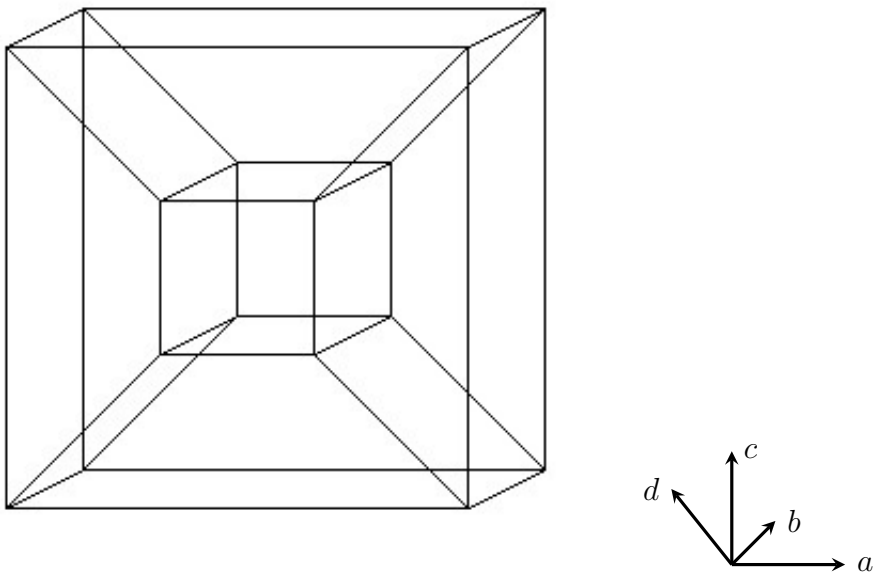


Figure 3: Hypercube for Problem 4(a).

Solution to Problem 4 (b)

Solution to Problem 4 (c)

Solution to Problem 4 (d)

Solution to Problem 4 (e)

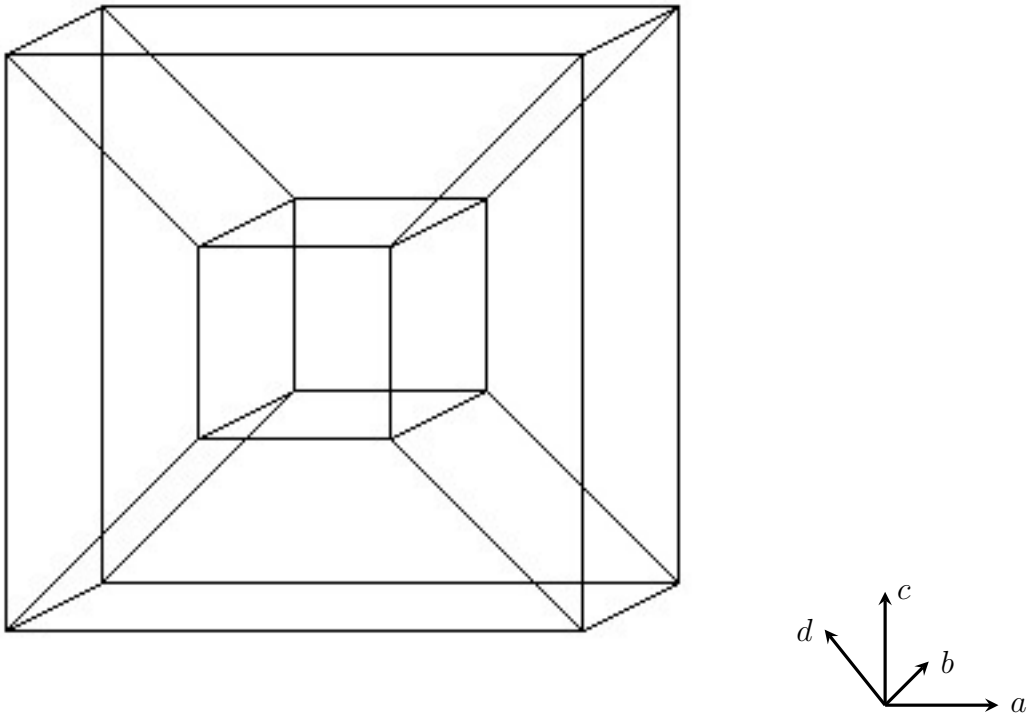


Figure 4: Supplementary hypercube for Problem 4(e).

Problem 5 – (25 pts)

Consider the data-flow graph for the following computation:

$$
\begin{aligned}
x_1 &= a \times b; \\
x_2 &= c \times d; \\
x_3 &= 13 \times x_1 + x_2; \\
x_4 &= 8 \times e; \\
x_5 &= x_3 + x_4; \\
x_6 &= 4 + x_5; \\
x &= (5 \times a) \times (x_6 \times b);
\end{aligned}
$$

where a, b, c, d, and e are inputs, and x is the final output.

All of the computations are to be completed in one clock cycle (i.e., operations in the data-flow graph cannot be shared). The area and delay of each available operators are listed as follows. Assume adders and multipliers have two inputs and shift operations take no area and no latency. *Note: you cannot use subtractors or other ALU operations.*

Operator	Area	Latency
Multiplier	4	3
Adder	1	2

(a) Draw the data-flow graph for the final output x using the operations as they appear in the expression, without any optimization. (3 pts)

(b) Apply behavioral-level optimization techniques to optimize the latency and area of the circuit and obtain the **two** Pareto points. Draw the optimized data-flow graphs and show the Pareto points in Figure 5. (20 pts)
Hint: start by balancing the graph to reduce the latency. Then, look for opportunities to reduce the area.

(c) Which of the Pareto points minimizes the area-delay product (i.e., the product of area and latency)? (2 pts)

Solution to Problem 5 (a)

Solution to Problem 5 (b)

Solution to Problem 5 (b) continued ...

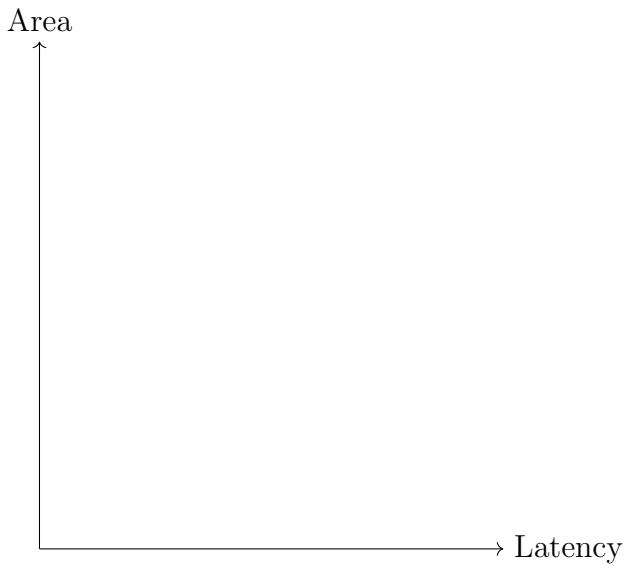


Figure 5: Area-latency trade-off plot.

Solution to Problem 5 (c)

The data-flow graph with area $A =$ _____ and latency $D =$ _____ has the smallest area-delay product $A \times D =$ _____.

Problem 6 – (10 pts)

Given the Boolean function $G = \bar{a} + ab\bar{c}\bar{d} + a\bar{b}c\bar{d}$, compute:

(a) The cofactor of G with respect to variable b. (2 pts)

(b) The cofactor of G with respect to variable $\bar{b}$. (2 pts)

(c) The Boolean difference $\partial G/\partial b$. (2 pts)

(d) The smoothing $S_b(G)$. (2 pts)

(e) The consensus $C_b(G)$. (2 pts)

Note: Minimize the expressions such that they have the minimum number of implicants and minimum number of literals for each implicant.

Solution to Problem 6 (a)

Solution to Problem 6 (b)

Solution to Problem 6 (c)

Solution to Problem 6 (d)

Solution to Problem 6 (e)