CS-472: Design Technologies for Integrated Systems

Exercise Problem Set 11 Date: 5/12/2024

Topics: Timing analysis & retiming (cf. slide sets 13 & 14)

Problem 1

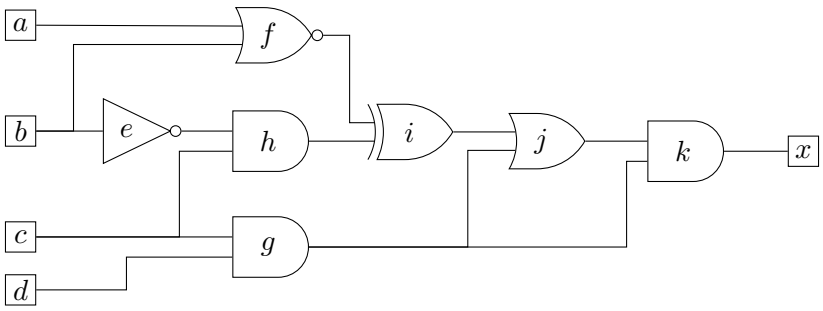

Figure 1: Combinational logic network.

Consider the network in Fig. 1: The inputs are $\{a, b, c, d\}$ and the output is x. The data ready time for all the inputs is 0, and the inputs are stable after time 0. Assume the following delays for logic gates:

INV gate: $t_d = 1$ ns;
AND gate: $t_d = 1$ ns;
OR/NOR/XOR gate: $t_d = 2$ ns.

(a) The data required time for the output x is 7 ns. Find all the topological critical paths.

(b) Is the path (b, e, h, i, j, k, x) a true critical path?

Problem 2

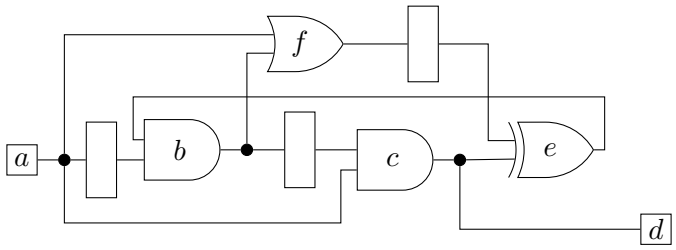

Figure 2: Sequential logic network.

Consider the network in Fig. 2, where the rectangles are registers. Assume the following delays for logic gates:

AND gate: $t_d = 3$ ns;
OR gate: $t_d = 4$ ns;
XOR gate: $t_d = 5$ ns.

(a) Draw the synchronous network graph, where weights of vertices are the combinational delays of the logic gates, and weights of the edges are the numbers of registers between two vertices.

(b) What is the minimum cycle time currently (before retiming)?

(c) Draw the constraint graph modeling to search for a legal retiming with a cycle time of 12 ns.

(d) To find a retiming solution, apply the Bellman-Ford Algorithm on the constraint graph using r_a as the source (compute the longest distance from r_a to each vertex).

(e) Redraw the retimed synchronous network graph using the retiming vector $\vec{r}$ obtained in (d). Verify that the targeted cycle time 12 ns is met.