CS-472: Design Technologies for Integrated Systems

Exercise Problem Set 10 Date: 21/11/2024

Topic: Boolean methods for multi-level logic synthesis (cf. slide set 12)

Problem 1

Consider the logic network where inputs are $\{a, b, c, d\}$ and output is $\{f\}$ defined as:

$$
\begin{aligned}
k &= ad \\
n &= c + k \\
m &= \overline{(ab)} \\
f &= m + n
\end{aligned}
$$

Assuming $CDC_{in} = ab$, compute CDC_{out}.

Problem 2

Consider the logic network from Problem 1. Compute the ODC sets for all internal and input vertices assuming that the output is fully observable.